U23ECT14 - Linear Integrated circuits

unit-1 - Basics of op-amp

IC Fabrication and circuit configuration for Linear ICs.

Advantages of ICs over discrete components

→ miniaturization and hence increased equipment density

→ cost reduction due to batch processing

→ Increased system reliability due to elimination of soldered joints

→ Improved functional performance

→ Matched devices

→ Increased operation speeds

→ Reduction in power consumption.

→ Extremely small in size

→ Less power consumption

→ Reliability is high.

→ Easy replacement

→ Battery operated system because of small power supply requirement.

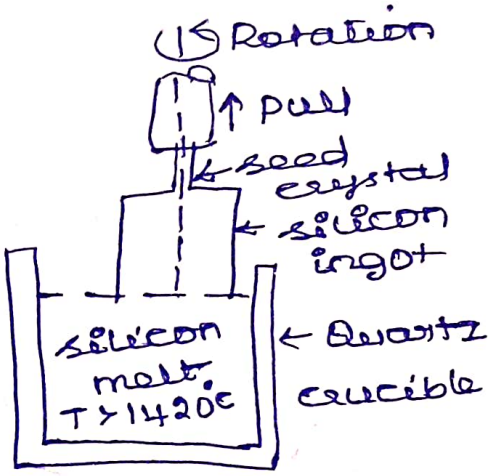
→ Greater ability to operating at extreme temperature.

Manufacturing process of monolithic ICs

→ silicon wafer preparation
→ Epitaxial growth
→ oxidation
→ photolithography
→ Metallization
→ Assembly processing and packaging
→ Diffusion
→ Ion Implantation
→ Isolation techniques

silicon wafer preparation

→ starting material for crystal growth is highly purified (99.999) polycrystalline silicon.



→ Czochralski crystal growth process — used for producing single crystal silicon ingots.

→ polycrystalline silicon together with an appropriate amount of dopants is put in a quartz crucible.

→ placed in furnace.

→ Heated upto temperature > 1420°C
↳ melting point of silicon.

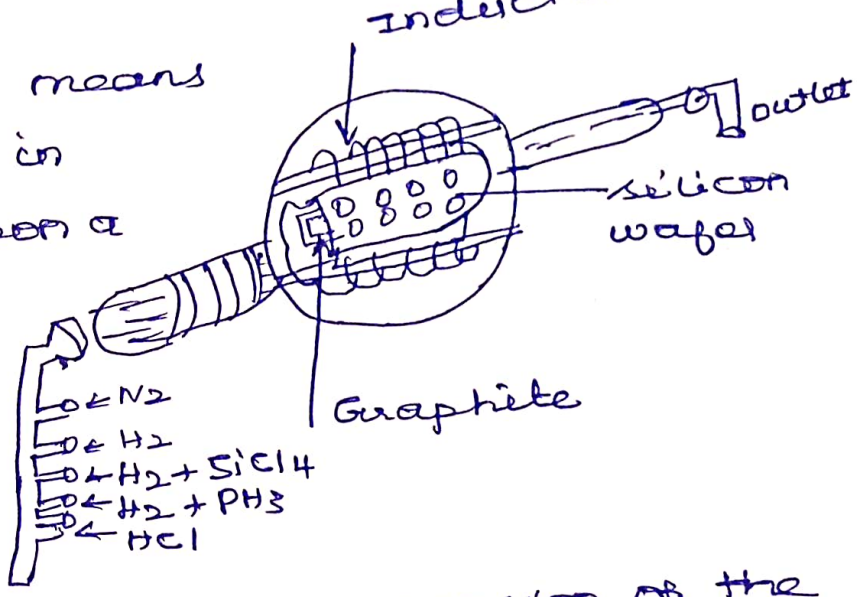
→ A small single crystal rod of silicon called a seed crystal is then dipped into the silicon melt slowly pulled up.

→ During crystal pulling operation the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross section.

→ The ingots are then cut into slices, about 100 thickness. It is about 10 to 15cm in common.

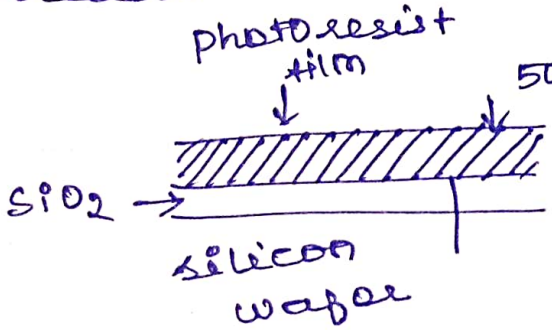
Epitaxial growth

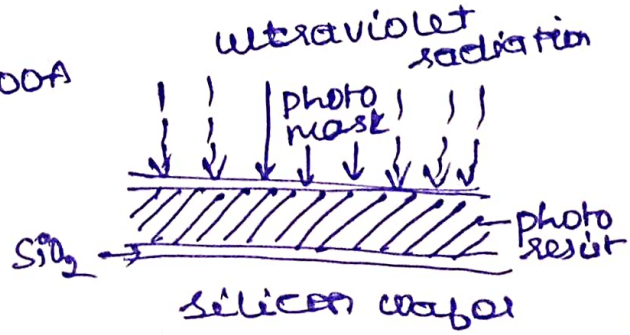
→ word epitaxy means arranging atoms in single crystal upon a single crystal structure, so that the layer is extended.



→ The structure is an extension of the original substrate.

→ The water is then rotated at a speed of 5000 rpm. So that photoresist spreads as thin coating over layer.





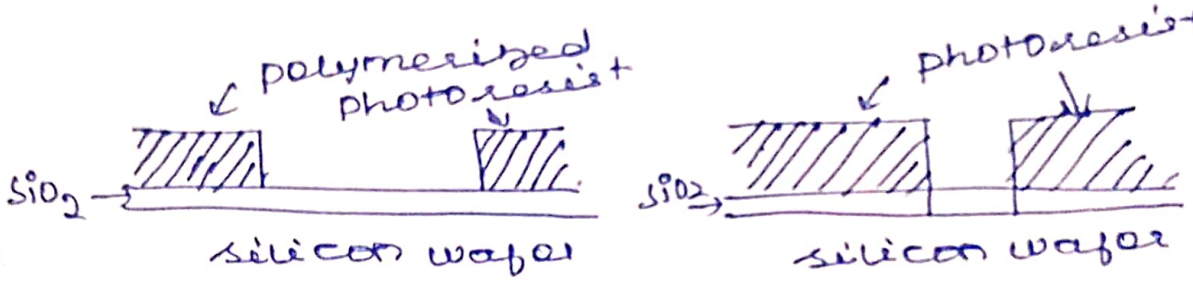
→ The next step is the photo mask over the water.

↳ It indicates the location of

windows where SiO_2 layer is removed.

→ The entire setup is then exposed to UV radiation.

↳ The transparent region of mask becomes polymerized.



→ Then the chip is dipped in the etching solution of hydrofluoric by the polymerized.

→ The basic reaction used for the epitaxial growth of pure silicon is

$$SiCl_4 + 2H_2 \underset{\longleftarrow}{\xrightarrow{1200^\circ C}} Si + 4HCl$$

→ The process is carried out in a reaction chamber consisting long cylindrical quartz table encircled by RF induction coil.

→ The Si wafer is placed on rectangular graphite rod called a boat. It is then placed in reaction chamber where, graphite is heated to $1200^\circ C$

Oxidation

→ SiO_2 has the property of preventing the diffusion of all impurities through it. It serves two important purpose.

→ SiO_2 is extremely hard protective coating and unaffected by moisture except hydrofluoric acid.

→ It acts as diffusion mask permitting selective diffusion into silicon water through etching SiO_2.

↳ used for insulating the metal interconnections from the silicon.

→ The water is exposed to gas °ᵢ containing O_2 or H_2O or both.

→ The chemical reaction is

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

→ This process is called thermal oxidation because high temperature °ᵢ used to grow the oxide layer.

→ The thickness in the order of 0.02 to 2 μm.

Photo Lithography:

→ with the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-waters.

→ As many of 10,000 transistors can be fabricated on 1 cm² chip.

→ It involves following process

↳ first step of photolithography is

applications of photoresist.

↳ It is light sensitive emulsion, which when exposion to UV rays and it becomes resistant to chemical corrosion.

→ The drop of photoresist is applied at the center of oxide layer.

Diffusion

→ Another important process is the diffusion of impurities in the silicon chip.

→ The diffusion process enables selective areas to be doped to required levels.

↳ p type semiconductor is obtained by diffusion of Boron in the form of solid, liquid or gaseous.

↳ N type semiconductor is obtained by diffusion of arsenic phosphorous.

→ The depth of diffusion depends upon the time of diffusion which extends to 2 hours.

Ion Implantation

→ It is other technique used to introduced impurities into a silicon wafer.

→ In this process, silicon wafers are placed in a vacuum chamber and are scanned by the beam of high energy dopant ions (Boron for

p type and phosphorus for N type)

→ The ions are accelerated by energies between 20kV to 250kV

→ As the ions strike the silicon wafer, they penetrate some small distance into the wafer.

→ The depth of penetration of any particular type of ion increases with increasing accelerating voltage.

Advantage.

↳ Low temperature

↳ Accelerating potential and the beam current are electrically controlled from outside.

Isolation techniques

→ since number of components are fabricated on the same IC, it becomes necessary to provide good isolation between various components and their interconnections.

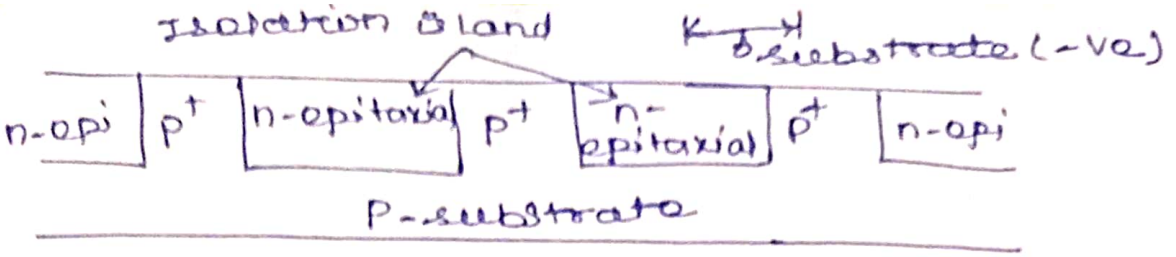
Two techniques.

→ PN junction isolation

→ Dielectric isolation.

PN Junction isolation

→ p type impurities are selectively diffused into the n type epitaxial layer so as to reach p type substrate at the bottom.

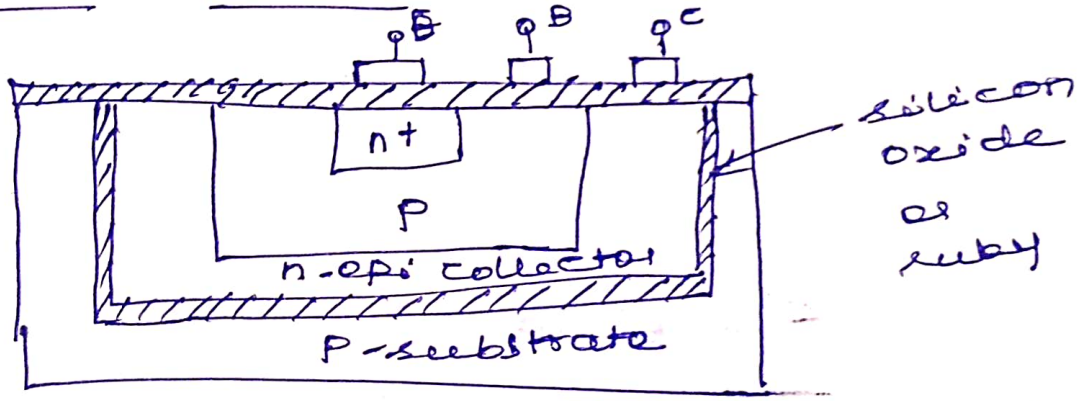


→ This produces islands surrounded by P type moats

→ If P-substrate is held at the most negative potential the diode becomes reverse biased, thus providing isolation between those islands.

→ This method is very economical and is the most commonly used Isolation method.

Dielectric isolation



→ Here a layer of solid dielectric such as silicon dioxide (or) ruby completely surrounds each components, thereby producing isolation, both electrical and physical.

→ It is possible to fabricate both npn & pnp transistor.

→ This method requires additional

fabrication stops, it becomes more expensive.

→ It is application of aerospace & military.

Metallization

→ The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip.

→ Aluminium is usually used for the metallization.

Advantages

↳ It is relatively a good conductor.

↳ It makes good mechanical bonds with silicon

↳ It is easy to deposit aluminium films using vacuum deposition.

↳ Aluminium forms low resistance, non rectifying contact with p type silicon and heavily doped n type silicon.

→ The metal leads are to be formed for making connections with the terminals of the devices.

→ Aluminium is deposited over the entire wafer by vacuum deposition.

→ Metalization is carried out by evaporating aluminium over the entire surface.

↳ Then selectively etching away aluminium to leave behind the desired interconnection and bonding pads.

Assembly processing and packaging

→ wafer in which, hundreds of ICs are fabricated. So these chips must be separated and individually packaged. A common method called scribing.

→ Individual chip cannot be directly handled because it is very small.

↳ Different package configuration

→ Metal can package

→ Flat package

→ Dual in line package.

Encapsulation

→ It is essential to protect it against mechanical and chemical damage while in use.

→ It is done by placing a cap over the circuit and sealing it in an inert atmosphere.

Basic operational Amplifier

→ operational Amplifier was introduced in 1947 by John. R. Ragazzini.

↳ To denote that a special type of amplifier, could be configured for a variety of operations such as amplification, addition, subtraction and integration.

Features:

→ multiterminal device.

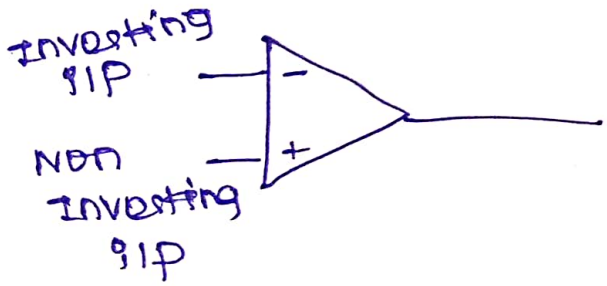
→ Internally is quite complex.

→ 2 input terminals and one output terminal.

→ (−) sign — Inverting ip terminal.

→ (+) sign — Non Inverting ip terminal.

Circuit Symbol



packages

→ Three popular packages.

↳ Metal can package

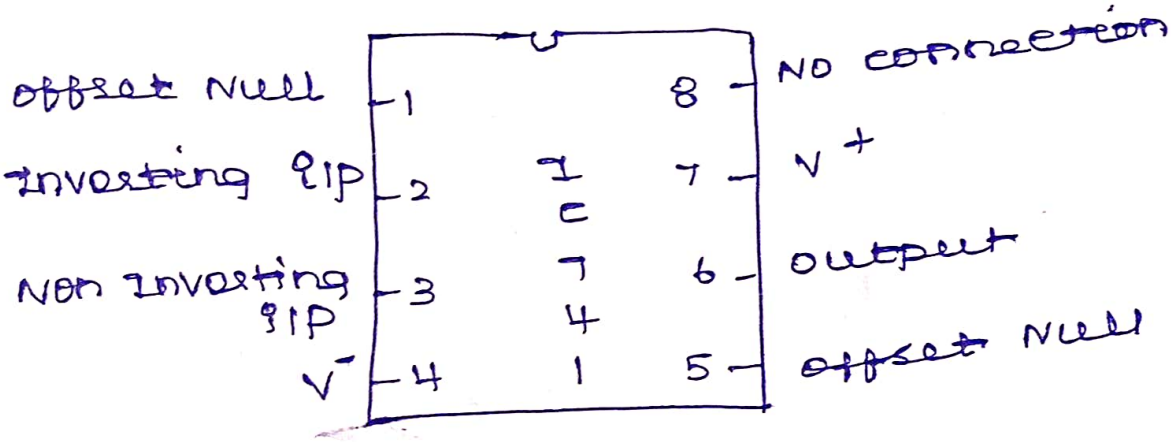
↳ dual in line package

↳ Flat package.

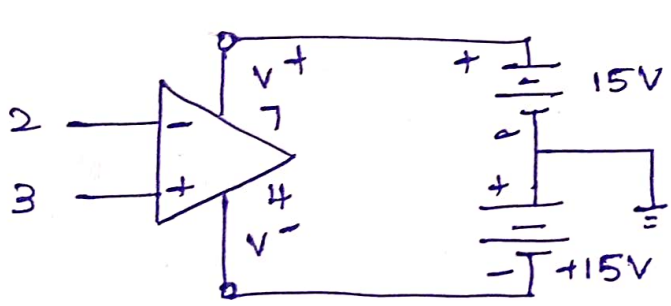
→ op amp packages may have single, two (dual) or four (quad) op amps.

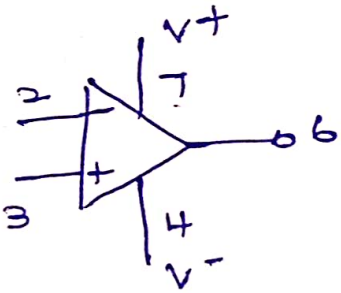
→ packages have either 8 or 10 or 14 terminals.

Op-Amp terminals (or) IC 741

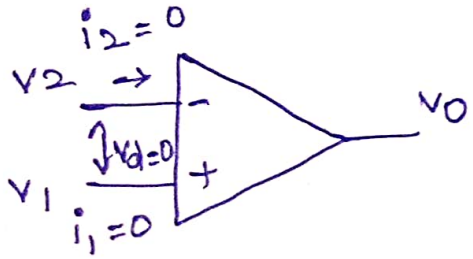


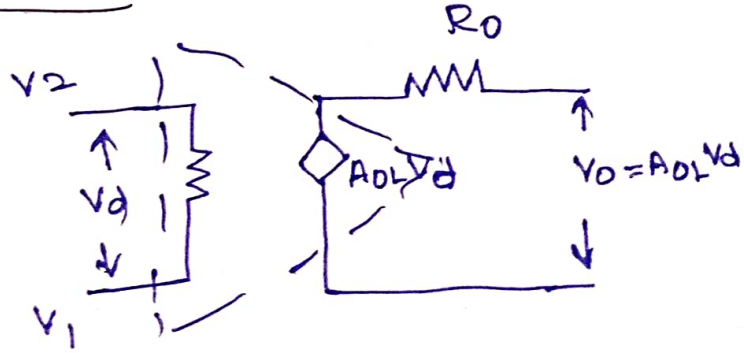
power supply connections





characteristics of op-amp





$V_1 = 0$, o/p → 180° out of phase with input signal V_2

$V_0 = 0$, o/p V_0 — In phase with the input signal at V_1 12

Open loop voltage gain, $A_{OL} = \infty$

Input Impedance, $R_i = \infty$

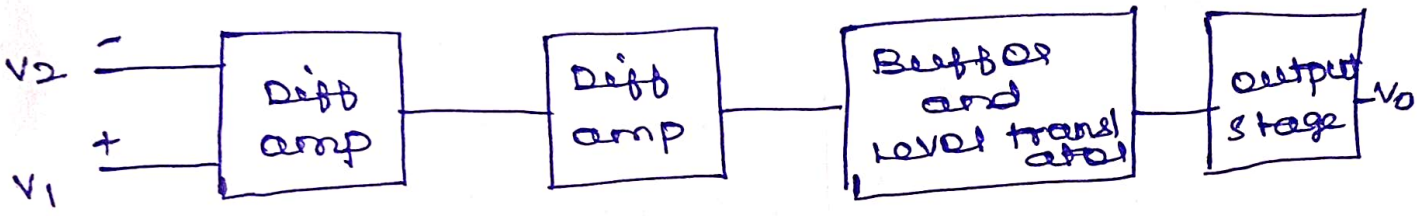
output Impedance, $R_o = 0$

Bandwidth, $BW = \infty$

Zero offset

ie, $V_o = 0$ when $V_1 = V_2 = 0$

Functional Block diagram



Input stage

→ provide high Input Impedance to prevent loading on the high gain stage.

→ Two Input terminals.

→ also requires low output Impedance.

→ All such requirements are achieved by using the dual I/P, balanced output differential amplifier as the I/P stage.

→ Differential amplifier is to amplify the difference between the two input signals.

→ has high Input Impedance.

→ It provides most of the voltage gain of the amplifier.

Intermediate stage

→ Another differential amplifier with dual Input, unbalanced.

→ Overall gain requirement of the op-amp is very high.

→ Input stage alone cannot provide such a high gain.

→ To provide an additional voltage gain required.

Level shifting stage

→ Level shifter brings the dc level down to ground potential, when no signal is applied at the Input terminal.

↳ The signal is given to the last stage which is the output stage.

→ Buffer is usually an emitter follower whose Input Impedance is very high.

↳ This prevents loading of the high gain stage.

Output stage

→ To provide low input impedance, large ac output voltage swing and high current sourcing and sinking capability.

→ The push pull complementary amplifier meets all these requirements and hence used as an output stage.

→ This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground.

AC and DC characteristics of op-amp

DC characteristics

→ Input bias current → Input offset current.

→ Input offset voltage → Thermal drift

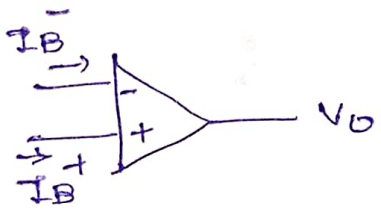
Input bias current

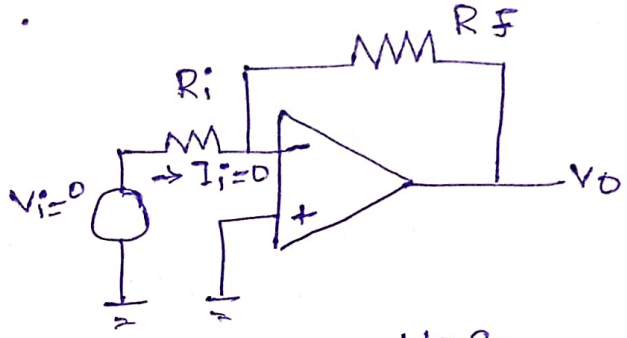
→ op amp's input is a differential amplifier, which may be made of BJT or FET

→ Input transistor must be biased into their linear region by supplying currents into the bases by the external circuit.

→ Ideal op-amp, no current is drawn

from input terminals.





→ Input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

→ current input bias current is the average value of the base entering into the input terminal of the op-amp

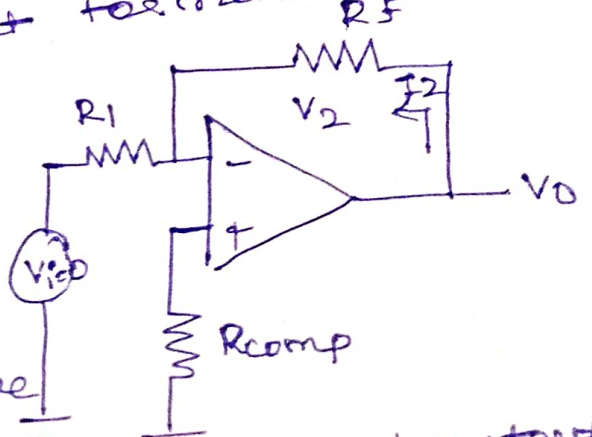
→ Input voltage V_i is to zero volts, V_o should be zero volts

$$V_o = (I_B^-) R_f$$

1 MΩ $V_O = 500\,nA \times 1\,M\Omega = 500mV$

→ output is driven to 500mV with zero input because of the bias current.

↳ This effect can be compensated resistor R_{comp} has been added between the non inverting input terminal and ground.



KVL:

$-V_1 + 0 + V_2 - V_O = 0$

$V_O = V_2 - V_1$

→ By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and output V_O will be zero.

The value of Rcomp is derived as

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

→ node 'a' is at voltage $(-V_1)$, because the voltage at the non inverting i/p terminal is $(-V_1)$ $V_i = 0$

$$I_1 = \frac{V_1}{R_1}$$

$$I_2 = \frac{V_2}{R_f}$$

$$I_{B2} = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right)$$

Assume $I_{B1} = I_{B2}$

$$\frac{V_1}{R_{comp}} = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right)$$

$$\boxed{R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \,||\, R_f}$$

Input offset current:

→ $I_{B1} = I_{B2}$ the bias current compensation

→ Input Resistance cannot be identical so always there exists a small difference between I_{B1} & I_{B2}

→ The difference in magnitude between I_{B1} & I_{B2}

$$I_{OS} = |I_{B1}| - |I_{B2}|$$

To find the effect of I_{OS} on V_O and assuming $V_i = 0$

$$V_1 = I_{B1} R_{comp} \qquad I_1 = \frac{V_{comp}}{R_1}$$

KCL, $I_2 = I_{B2} - I_1 = I_{B2} - I_{B1} \frac{R_{comp}}{R_1}$

$$V_O = I_2 R_F - V_{com} = I_2 R_F - I_{B1} R_{comp}$$

$$= \left(I_{B2} R_f - I_{B1} \frac{R_{comp}}{R_1} - I_{B1} R_{comp} \right)$$

$$= I_{B2} R_f - I_{B1} \frac{R_{comp}}{R_1} \cdot \frac{R_F R_1}{R_1 + R_F} -$$

$$I_{B1} \left(\frac{R_F R_1}{R_1 + R_F} \right)$$

$$= I_{B2} R_F - I_{B1} \cdot \frac{R_F}{R_1 + R_F} (R_F + R_1)$$

$$V_O = R_F (I_{B2} - I_{B1})$$

$$\boxed{V_O = R_F I_{OS}}$$

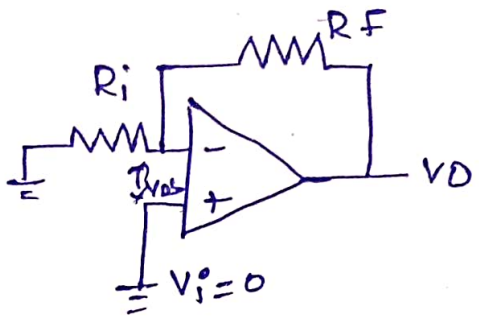
Input offset voltage

→ voltage that is to be applied between the two input terminals for making the output voltage zero.

$$V_a = V_o \left(\frac{R_1}{R_1 + R_F} \right)$$

$$V_o = V_a \frac{(R_1 + R_F)}{R_1}$$

$$= \left(1 + \frac{R_F}{R_1} \right) V_a$$



$V_{OS} = V_i - V_a$ and with $V_i = 0$

$$V_{OS} = -V_a = |V_a|$$

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1} \right) V_{OS}}$$

Output offset voltage

→ Total output voltage can be either the input bias current or the input offset and also it can be either positive or negative with respect to ground.

$$V_{OT} = \left(1 + \frac{R_f}{R_1} \right) V_{OS} + R_f I_B$$

$$\boxed{V_{OT} = \left(1 + \frac{R_f}{R_1} \right) V_{OS} + R_f I_{OS}}$$

Thermal drift

→ Bias circuit offset current and offset voltage with temperature.

→ The average rate of change of input offset voltage per unit change in temperature.

$$\text{Thermal drift} = \frac{\Delta I_{OS}}{\Delta T} \text{ in V/C}$$

AC characteristics

→ op-amp is used in a circuit for amplifying,

↳ frequency response

↳ slew rate.

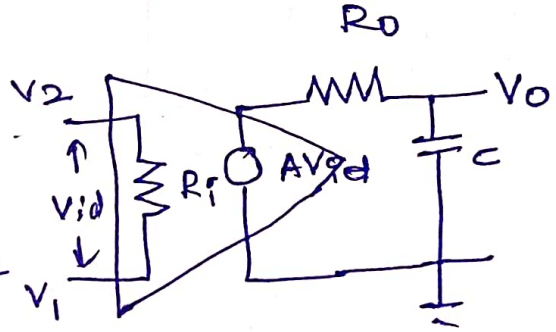
Frequency response

→ defined as the manner in which the gain of the op-amp responds different frequencies.

→ Any change in the operating frequency causes variation in which the magnitude and phase angle.

Open loop

→ There is one break frequency by c at the output.

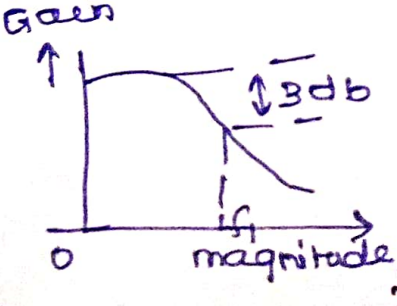


$$V_O = \frac{1/j\omega C}{R_O + 1/j\omega C} A_O V_{id}$$

$$\text{Gain } A = \frac{V_O}{V_{id}} = \frac{A_O}{1 + j(F/F_1)} \quad \text{if } F_1 = \frac{1}{2\pi R_O C}$$

$$A = \frac{A_O}{1 + j(F/F_1)}$$

$$|A| = \frac{A_O}{\sqrt{1 + (F/F_1)^2}}$$



$$\theta = \tan^{-1}\left(\frac{F}{F_1}\right)$$

Characteristics

→ $F << F_1$ → gain is $20 \log A_0$ in db

→ $F = F_1$ → gain is 3 db down from the dc level

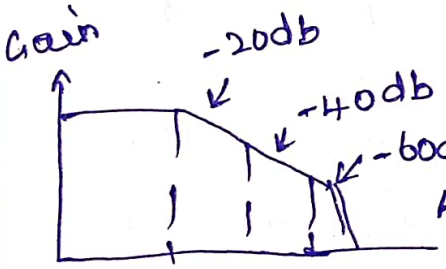
→ $F >> F_1$ → gain rolls off at −20 db.

Transfer function

$$A = \frac{A_0}{1 + j(F/F_1)} = \frac{A_0}{1 + j(\omega/\omega_1)}$$

$$A = \frac{A_0 \omega_1}{\omega_1 + j\omega} = \frac{A_0 \omega_1}{s + \omega_1}$$

$$A = \frac{A_0}{(1 + jF/F_1)(1 + jF/F_2)(1 + jF/F_3)}$$



$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

Closed loop frequency response

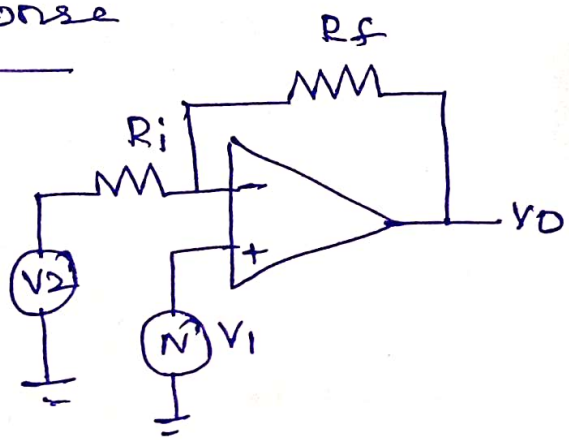
Transfer function

$$A_V = \frac{A_0}{1 + A_0\beta}$$

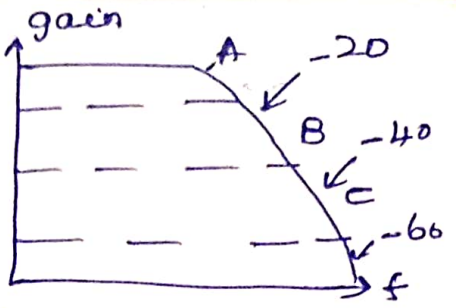
$$1 + A_0\beta = 0$$

$$A_V = \frac{A_0}{1 - (-A_0\beta)}$$

$-A_0\beta = 1$ magnitude



$$\text{Gain } A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$



closed loop transfer function given by

use of $1 + A\beta = 0$

$$1 + \frac{A_0 \beta \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$$

Frequency compensation

→ used for large bandwidth and lower closed loop gain.

↳ External compensation

↳ Internal compensation

External compensation

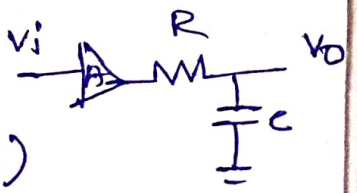
→ compensation network alters the open loop gain so the roll off rate is -20db/decade over wide range of frequency

↳ Dominant pole compensation

↳ pole zero compensation.

Dominant pole compensation

$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$



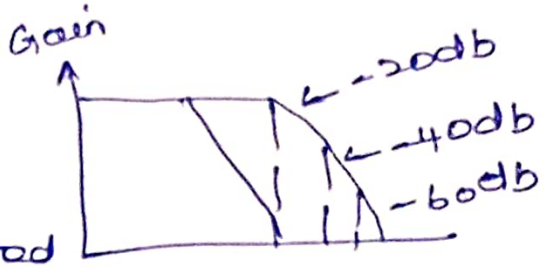
compensated transfer function 'A'

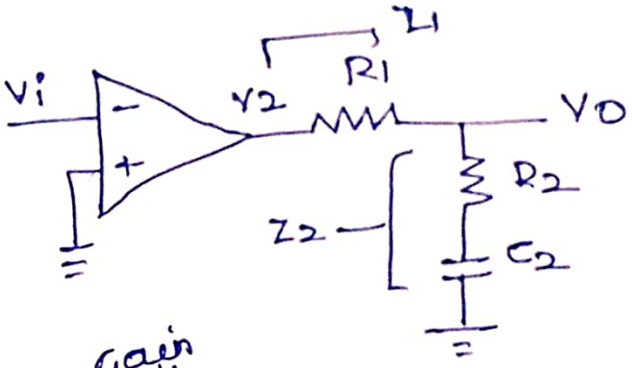
$$A' = \frac{V_0}{V_i} = A_0 = \frac{(1+j\omega_c)}{R+1/j\omega_c} = \frac{A_0}{1+j(f/f_d)}$$

$$A' = \frac{A_0}{(1+jF/F_d)(1+jF/F_1)(1+jF/F_2)} \qquad F_d = \frac{1}{2\pi RC}$$

pole zero compensation

→ pole and zero are added to the uncompensated transfer function.

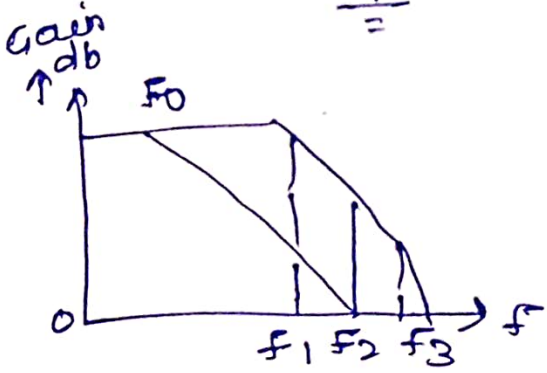




$$\frac{V_0}{V_2} = \frac{Z_2}{Z_1 + Z_2}$$

$$= \frac{R_2 + 1/j\omega C_2}{R_1 + R_2 + 1/j\omega C_2}$$

$$F_1 = \frac{1}{2\pi R_2 C_2}$$



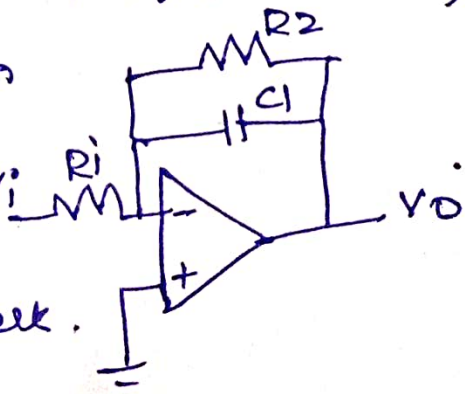
$$F_2 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

$$A' = \frac{1+j(F/F_1)}{(1+jF/F_0)} \cdot \frac{A_0}{(1+jF/F_0)(1+jF/F_2)(1+jF/F_3)}$$

$$A' = \frac{A_0}{(1+jF/F_0)(1+jF/F_2)(1+jF/F_3)}$$

Miller effect compensation

→ C_1 parallel with R_2 the combination of R_1 & C_1 behaves as phase lead network.

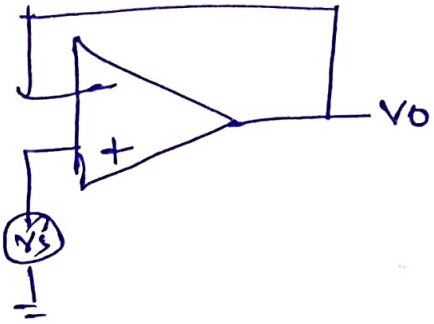


Slew Rate

→ maximum rate of change of output voltage with time

$$S = \frac{dV_o}{dt}$$

→ Input wave is applied to the circuit both distorted output.



$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

Rate of change of output $\frac{dV_o}{dt} = \frac{d}{dt}(V_m \sin \omega t)$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

→ maximum rate of change of output occurs when $\cos \omega t = 1$

$$\text{slew rate} = \left.\frac{dV_o}{dt}\right|_{max} = V_m \cdot \omega$$

→ maximum frequency at which distorted less output with peak value

$$f_{max} = \frac{\text{Slew rate}}{2\pi m}$$

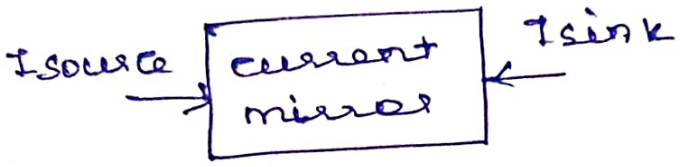
→ maximum peak voltage

$$V_{m(max)} = \frac{\text{slew rate}}{2\pi f}$$

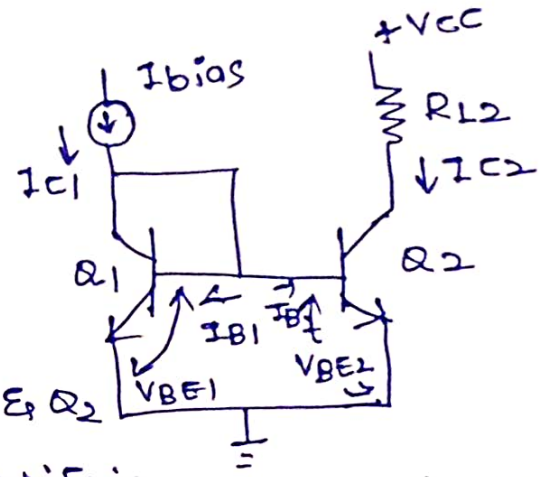
Current Mirror

→ The circuit in which the output current is forced to equal the input current.

→ Output current is the mirror image of input current.

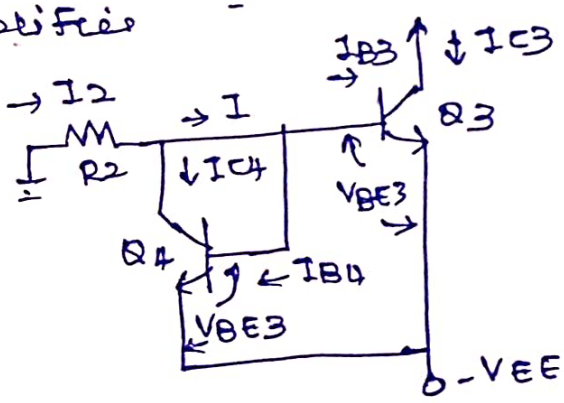


$I_{source} = I_{sink}$



→ To the emitter of Q_1 & Q_2 of differential amplifier

→ Base emitter voltage and base currents are same.



$V_{BE3} = V_{BE4}$

$I_{B3} = I_{B4}$

II(y) the collector current are also same

$I_{C3} = I_{C4}$

$I_2 = I + I_{C4}$

$I = I_{B3} + I_{B4} = 2I_{B3} = 2I_{B4}$

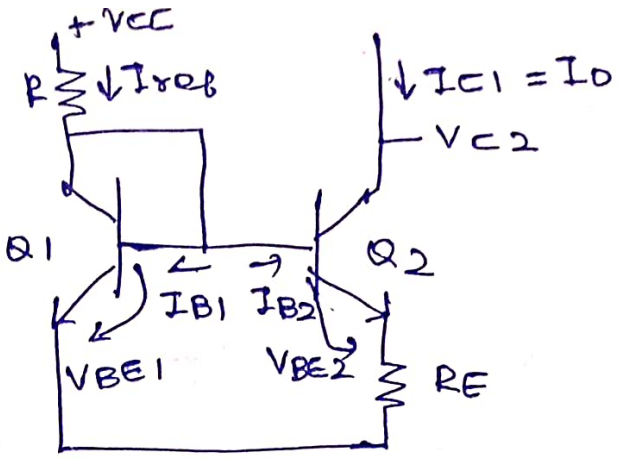
$I_2 = 2I_{B3} + I_{C4} = 2I_{B4} + I_{C4}$

$$I_{B3} = \frac{I_{C3}}{\beta}$$

$$I_2 = I_{C3} + \frac{2I_{C3}}{\beta}$$

$$I_2 R_2 - V_{BE3} + V_{EE} = 0 \quad , \quad I_2 = \frac{V_{BE} - V_{BE3}}{R_2}$$

Widlar current source



→ Two transistors Q1 and Q2 are identical but due to emitter resistance RE, VBE1 & VBE2 are different.

$V_{BE2} < V_{BE1}$ and $I_{C1} < I_{C2}$

KVL:

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_E$$

$$V_{BE1} - V_{BE2} = (I_{B2} + I_{C2}) R_E$$

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = I_S e^{\frac{V_{BE2}}{V_T}}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_S e^{\frac{V_{BE1}}{V_T}}}{I_S e^{\frac{V_{BE2}}{V_T}}}$$

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T}$$

Take natural log on both side.

$$\ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{V_{BE1} - V_{BE2}}{V_T}$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$(I_{B2} - I_{C2}) R_E = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

Large value of β, I_{B2} is neglecting

$$I_{C2} R_E = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$V_{BE1} = V_{BE2} + V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$= V_{BE2} + (I_{B2} + I_{C2}) R_E$$

$$V_{BE1} - V_{BE2} = \left(\frac{I_{C2}}{\beta_2} + I_{C2}\right) R_E$$

$$V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) = \left(1 + \frac{1}{\beta_2}\right) R_E$$

$$R_E = \frac{V_T}{1 + 1/\beta_2} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

KVL at node 'a'

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$= I_{C1}\left(1 + \frac{1}{\beta_1}\right) + \frac{I_{C2}}{\beta_2}$$

$\beta_1 = \beta_2 = \beta$

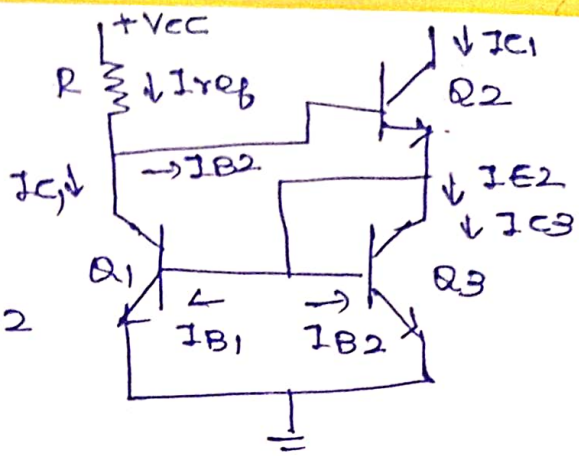
$$I_{ref} = I_{C1}\left(1 + \frac{1}{\beta}\right) = I_{C1}\left(\frac{1+\beta}{\beta}\right)$$

$$\boxed{I_{C1} = I_{ref}\left(\frac{\beta}{1+\beta}\right)}$$

$$I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1}$$

$\beta >> 1$, $I_O = I_{C2} = I_{ref}$

Wilson Current Source



KVL

$$I_{ref} = I_{B2} + I_{C1}$$

$$I_{E2} = I_{C3} + I_{B1} + I_{B2}$$

Identical transistor

Q_1, Q_2 & Q_3

$$V_{BE1} = V_{BE2} = V_{BE3}$$

$$I_{B1} = I_{B2} = I_{B3} = I_B$$

$$I_{E2} = I_{C3} + 2I_B$$

$$I_{E2} = I_{C2} + I_B$$

$$I_{C2} = I_{E2} - I_B$$

$$= I_{C3} + 2I_B - I_B$$

$$= I_{C3} + I_B$$

$I_{C3} + I_{C1}$ as transistor are identical

$$I_{C2} = I_{C1} + I_B$$

$\therefore I_2 = I_{C2} = I_{ref}$

$$I_{E2} = I_{C3} + 2I_B$$

$$I_B = \frac{I_{C3}}{\beta}$$

$$I_{E2} = I_{C3} + \frac{2I_{C3}}{\beta} = I_{C3}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C2} = I_{E2}\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C2} = I_{C3}\left(1 + \frac{2\beta}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C3} = I_{C2}\ \frac{1}{(1+2/\beta)\left(\beta/1+\beta\right)}$$

$$I_{C1} = I_{ref} - I_B$$

$$= I_{ref} - \frac{I_{C2}}{\beta}$$

$$I_{C3} = I_{C1}$$

$$I_{C3} = I_{ref} - \frac{I_{C2}}{\beta}$$

$$I_{ref} - \frac{I_{C2}}{\beta} = I_{C2} \frac{1}{\left(1+\frac{2}{\beta}\right)\left(\beta/1+\beta\right)}$$

$$I_{ref} = \frac{I_{C2}}{\left(\frac{\beta+2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} + \frac{I_{C2}}{\beta}$$

$$= I_{C2}\left(\frac{1+\beta}{2+\beta} + \frac{1}{\beta}\right)$$

$$= I_{C2}\left[\frac{\beta(1+\beta)+2+\beta}{\beta(2+\beta)}\right] + I_{C2}\left[\frac{\beta+\beta^2+2+\beta}{\beta(2+\beta)}\right]$$

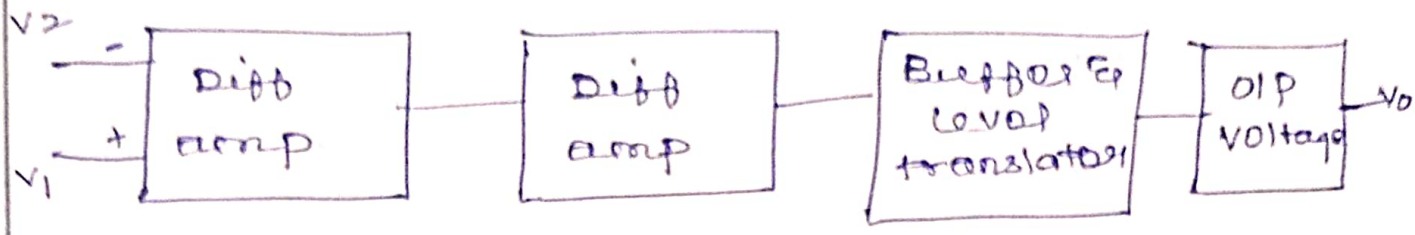
$$I_{ref} = I_{C2}\left(\frac{\beta^2+2\beta+2}{2\beta+\beta^2}\right)$$

$$I_{C2} = \frac{I_{ref}(\beta^2+2\beta)}{\beta^2+2\beta+2} = \frac{I_{ref}(\beta^2+2\beta+2-2)}{\beta^2+2\beta+2}$$

$$\boxed{I_{C2} = I_{ref}\left(1 - \frac{2}{\beta^2+2\beta+2}\right)}$$

$I_{C2} = I_2$ and I_{ref} differ by only the factor which is the order of $2/\beta^2$.

General operational Amplifier Stage and Internal circuit Diagram of IC 741.



→ The first two stages are cascaded differential amplifier and are designed to provide high gain and high input resistance.

→ The third stage acts as a buffer and as well as level shifter.

→ The buffer is usually and emitter follower whose input impedance is very high, so that it prevents loading.

→ The level shifter adjust the DC voltage so, that the output voltage is zero for zero inputs.

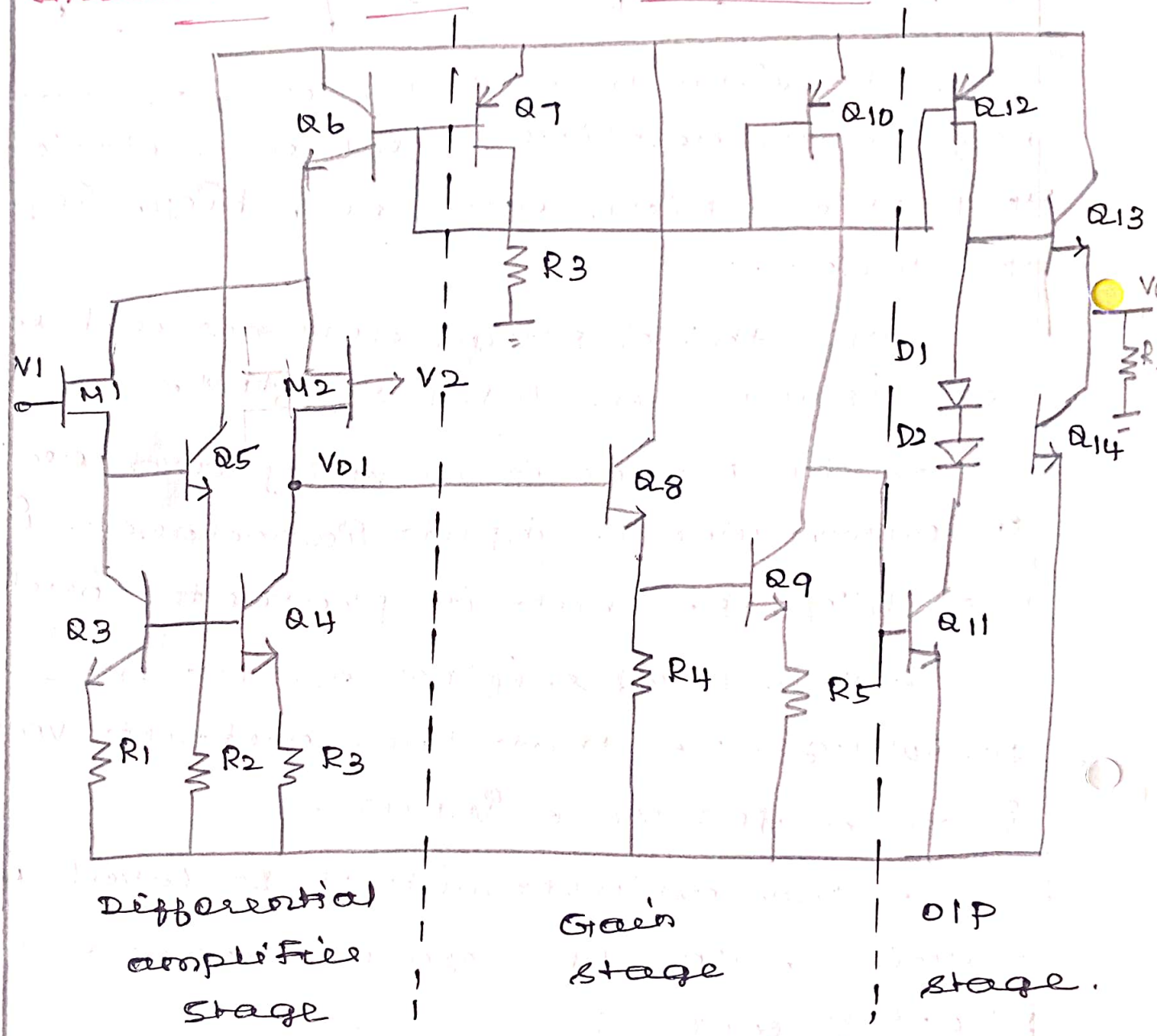
→ The adjustment of DC level is required for the gain stages are Directly coupled.

→ The output stage is desired to provide low output impedance.

→ The output voltage should seeing symmetrically with respect to ground.

→ TO allow such symmetrical swing the operand provided with both positive and negative supply voltage.

Internal circuit diagrams of IC 741



→ op-amp generally consists of three stage.

↳ Input stage

↳ Gain stage

↳ output stage

Input stage:

→ Differential amplifier stage was p channel JFET's M1 & M2.

→ Three transistor active load formed Q3, Q4, Q5

→ Q6, Q7 - used as bias current.

→ R1 is the output resistance looking into the collector of Q4

↳ Indicated by R_{O4}.

↳ Increases the stability.

→ A single ended output is taken at the collector of Q4.

Gain stage:

→ uses darlington transistor pair formed by Q8 & Q9.

→ Q8 - connected as emitter follower.

↳ providing large input resistance.

↳ To minimize the loading effect.

→ Q9 → provides an additional gain

↳ Q10 - acts as an active load.

→ Q7 & Q10 - establishes the bias current for Q9.

Output stage:

→ class AB complamentary push pull output stage.

→ Q11 → Emitter follower.

↳ To provide Larger input resistance.

→ Bias current for Q11

↳ provided by current mirror

↳ Q7 & Q12 → through diodes D1 & D2

→ Overall gain - this operational amplifier

$$A_V = |A_d||A_2||A_3|$$

A_d - Gain of differential amplifier

A_2 - Gain of gain stage

A_3 - Gain of output stage

open and closed loop configurations:

open loop op-amp configuration

→ The open loop indicates that no feedback path is no signal fed to the input from output.

configuration

↳ Differential amplifier

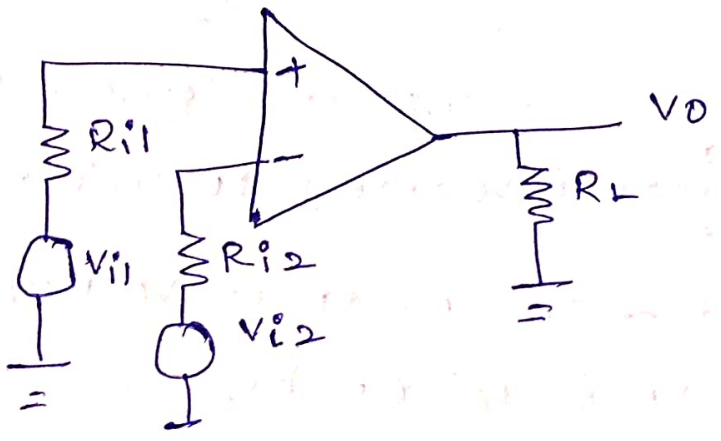
↳ Inverting amplifier

↳ Non inverting amplifier.

Differential amplifier

→ Input is applied to both the inverting and non inverting terminal of op-amp.

→ It amplifies the difference between two input voltages.



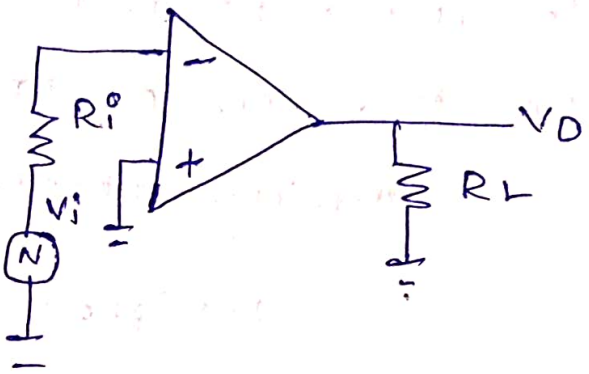
→ Input voltage $V_o = A V_{i1} V_{i2}$

→ the output voltage $\boxed{V_o = A(V_{i1} - V_{i2})}$

Inverting amplifier

→ Input applied to the inverting terminal only and non inverting terminal is ground.

→ The output voltage is 180° out of phase with its input signal



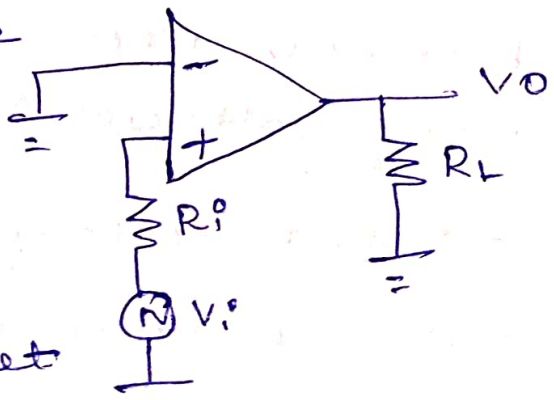
$$V_O = -AV_i$$

→ It indicates input signal V_i is amplified by open loop gain and is phase shifted 180° denoted as -Ve sign of output.

Non Inverting amplifier

→ Input signal is applied to the non inverting terminal is grounded.

→ The output voltage V_O is given by



$$V_O = AV_i$$

→ It indicates input signal V_i is amplified by open loop gain and is in phase with its input denoted as +Ve sign of output.

closed loop configuration

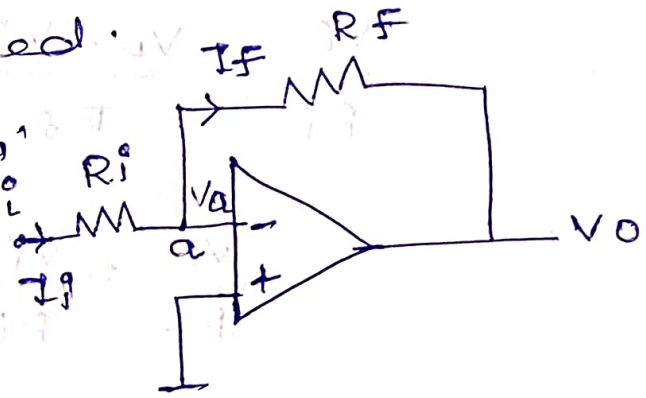
→ The closed loop indicates that there is a feedback path between output and input some signal of the output fed back to the input is called closed loop configuration.

configuration

- ↳ Inverting amplifier
- ↳ Non Inverting amplifier
- ↳ Differential amplifier.

Inverting amplifier

→ Input is given to the inverting terminal of op amp and non inverting terminal is grounded.



Apply KCL at node 'a'

$I_1 = I_f$

$$\frac{V_i - V_a}{R_i} = \frac{V_a - V_o}{R_f}$$

$V_a = 0$

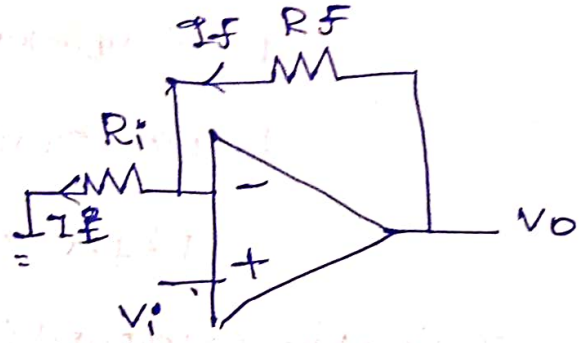
$$\frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$\boxed{V_o = -\frac{R_f}{R_i} V_i}$$

$$\text{gain } A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

Non Inverting amplifier

→ Input is given to the non inverting terminal and inverting terminal is grounded.



→ KCL at node 'a'

$$I_i = I_f$$

$$\frac{V_a - 0}{R_i} = \frac{V_o - V_a}{R_f} \qquad V_a = V_i$$

$$\frac{V_i}{R_i} = \frac{V_o - V_i}{R_f} \Rightarrow \frac{V_i}{R_i} = \frac{V_o}{R_f} - \frac{V_i}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_i}{R_i} + \frac{V_i}{R_f}$$

$$= V_i \left(\frac{1}{R_i} + \frac{1}{R_f} \right)$$

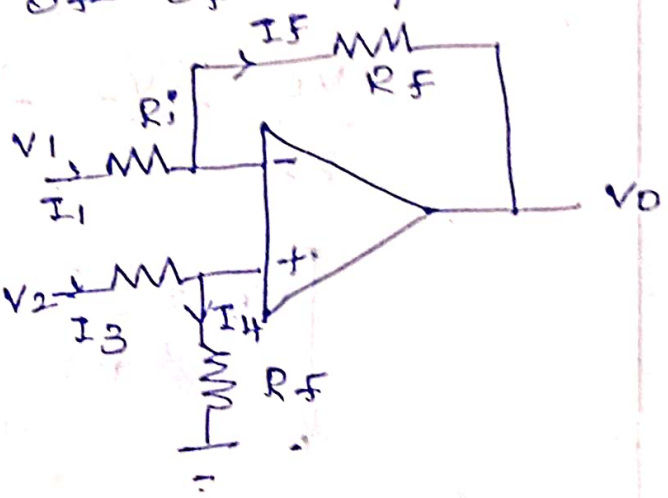
$$\frac{V_o}{R_f} = V_i \left(\frac{R_f + R_i}{R_i R_f} \right)$$

$$V_o = V_i R_f \left(\frac{R_f + R_i}{R_i R_f} \right)$$

$$\boxed{V_0 = V_i\left(1 + \frac{R_f}{R_i}\right)}$$

Differential amplifier:

→ Input is given the both Inverting and non Inverting of op-amp



KCL at node a.

$I_1 = I_2$

$$\frac{V_1 - V_3}{R_1} = \frac{V_3 - V_0}{R_f}$$

$$\frac{V_1}{R_1} - \frac{V_3}{R_1} = \frac{V_3}{R_f} - \frac{V_0}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_3}{R_f} + \frac{V_3}{R_1} - \frac{V_1}{R_1}$$

Inverting terminal

$$-\frac{V_0}{R_f} = \frac{V_1}{R_1} - V_3\left(\frac{1}{R_f} + \frac{1}{R_1}\right)$$

Apply KCL at node b

$I_3 = I_4$

$$\frac{V_2 - V_3}{R_1} = \frac{V_3 - 0}{R_f}$$

$$\frac{V_2}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = 0$$

$$\frac{V_2}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_F}\right)$$

$$-\frac{V_O}{R_F} = \frac{V_1}{R_1} - \frac{V_2}{R_1}$$

$$\frac{V_O}{R_F} = \frac{V_2}{R_1} - \frac{V_1}{R_1}$$

$$\boxed{V_O = \frac{R_F}{R_1}(V_2 - V_1)}$$

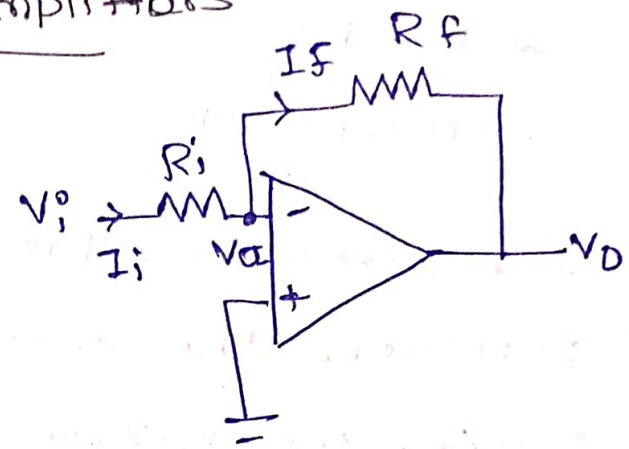
$$V_O = A_{CL}(V_2 - V_1)$$

$$\boxed{\text{Gain} = A_{CL} = \frac{V_O}{V_2 - V_1}}$$

Unit - 2

Applications of operational Amplifiers

Inverting amplifier



KCL,

$$I_i = I_f$$

$$\frac{V_i - V_a}{R_i} = \frac{V_a - V_o}{R_f}$$

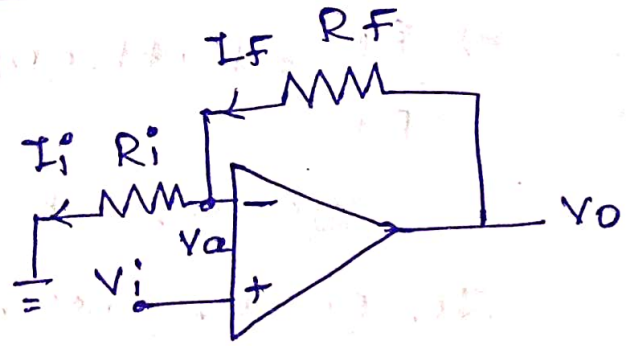
$\boxed{V_a = 0}$ virtual ground

$$\frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$V_o = -\frac{R_f}{R_i} V_i$$

$$\boxed{A = \frac{V_o}{V_i} = -\frac{R_f}{R_i}}$$

Non Inverting amplifier



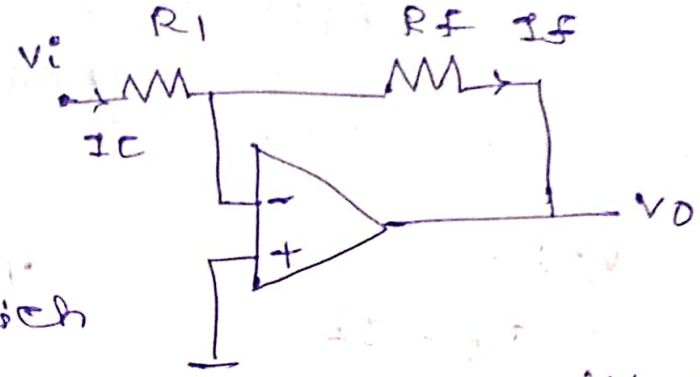
$$I_1 = I_f$$

$$\frac{V_a - 0}{R_i} = \frac{V_o - V_a}{R_f}$$

$\boxed{V_a = V_i}$ virtual ground

$$\frac{V_i}{R_i} = \frac{V_o - V_i}{R_f}$$

Sign changer



→ $R_i = R_f$

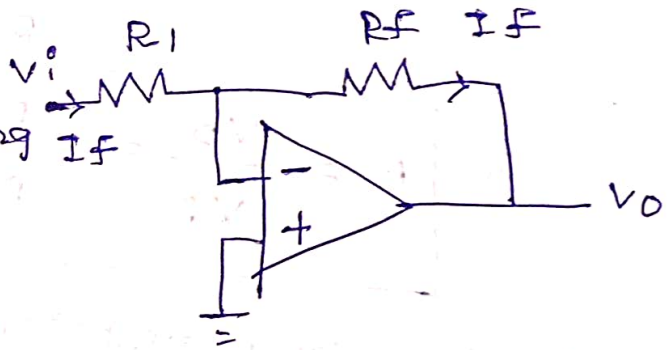
→ gain = −1

→ A circuit which produces the output signal with the same magnitude of the input signal but out of phase.

$$V_o = -\frac{R_f}{R_1} V_i$$

$R_f = R_i$, $\boxed{V_o = -V_i}$

Scale changer



→ consider inverting amplifier.

→ $\frac{R_f}{R_1} = k$, then

gain = −k

In scale changer, the output is some constant factor multiplication of i/p signal

$$\frac{R_f}{R_1} = k, \quad R_f = kR_1$$

$$V_o = -\frac{R_f}{R_1} V_i \quad \boxed{V_o = -kV_i}$$

$$\frac{V_i}{R_i} = \frac{V_o}{R_f} - \frac{V_i}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_i}{R_i} + \frac{V_i}{R_f}$$

$$\frac{V_o}{R_f} = V_i \left(\frac{R_f}{R_i} + \frac{R_f}{R_f} \right)$$

$$A = \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i} \right)$$

V to I converters

→ transconductance amplifiers.

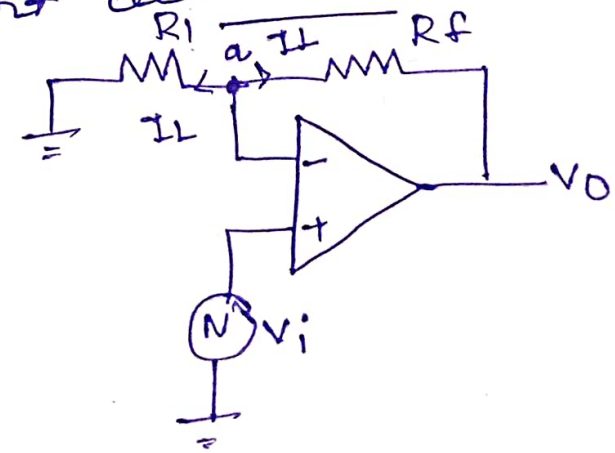
→ output current is proportional to the input voltage.

Two types

↳ voltage to current with floating load

↳ voltage to current with grounded load.

voltage to current with floating Load



node a is V_i

$I_B = 0$

$V_i = R_1 I_L$

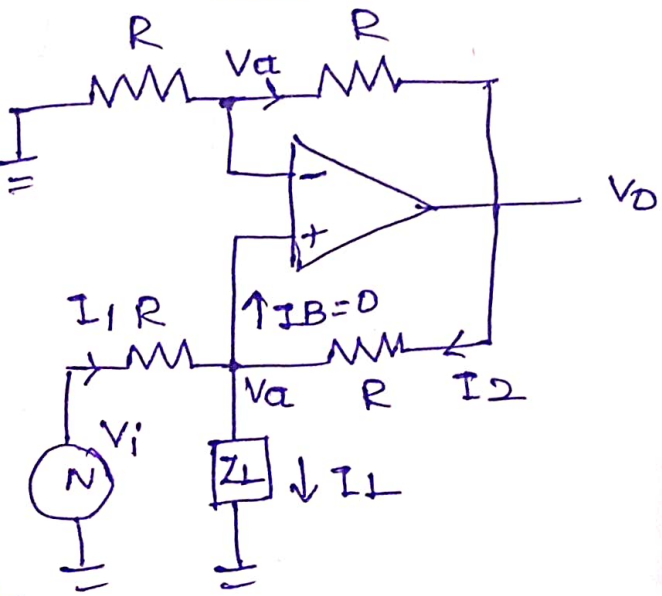
$$I_L = \frac{V_i}{R_1}$$

$$I_L = kV_i \qquad \therefore \frac{1}{R_1} = k$$

$$\boxed{I_L \propto V_i}$$

Input voltage is converted into an output current I_L.

Voltage to current with Grounded load



→ Voltage at node 'a' is Va

Apply KVL at node a

$$I_1 + I_2 = I_L$$

$$\frac{V_i - V_a}{R} + \frac{V_o - V_a}{R} = I_L$$

$$V_i - V_a + V_o - V_a = I_L R$$

$$V_i + V_o - 2V_a = I_L R$$

$$\boxed{V_a = \frac{-I_L R + V_i + V_o}{2}}$$

OP-amp is non inverting amplifier

$$A_V = 1 + \frac{R}{R} = 1 + 1 = 2$$

$$A_V = \frac{V_O}{V_a} = 2 \qquad V_O = 2V_a$$

$$V_O = \alpha \left[\frac{V_i + V_O - RI_L}{\alpha} \right]$$

$$V_O = V_i + V_O - RI_L$$

$$I_L = \frac{V_i}{R}$$

$$\therefore \frac{1}{R} = k$$

$$I_L = V_i k$$

$$\boxed{I_L \propto V_i}$$

$$\text{transconductance } (g_m) = \frac{I_L}{V_i} = \frac{1}{R}$$

$$\boxed{I_L = V_i g_m}$$

current to voltage converter

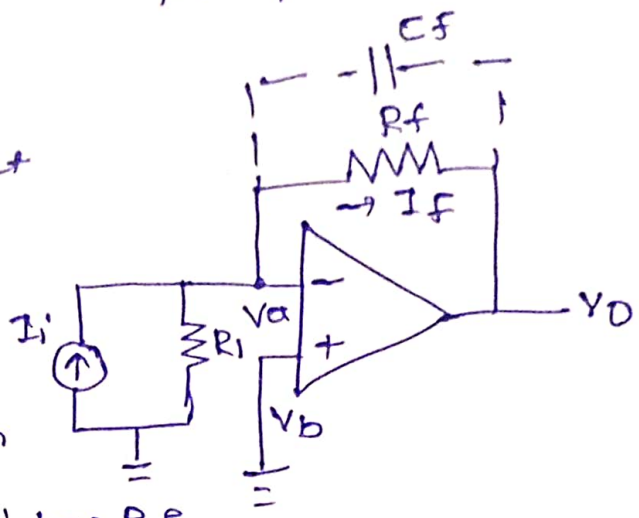
→ Ideal current controlled voltage source also called transresistance amplifier.

↳ output voltage is equal to a constant k times the magnitude of an independent I_i

$$\boxed{V_O = kI_i}$$

↳ o/p voltage is independent of the load connected it to.

→ output voltage is proportional to the input current



→ Va = 0, the current through R_1 is zero

→ I_i flows through the feedback resistor R_f

$$V_a = -I_i R_f$$

→ C_f connected across R_f. It is used to reduce high frequency noise

Input current $I_i = \frac{V_i - V_o}{R_f} = -\frac{V_o}{R_f}$ $V_i = 0$

$$I_i = -\frac{V_o}{R_f}$$

$$V_o = -I_i R_f$$

$$\boxed{V_o \propto I_i}$$

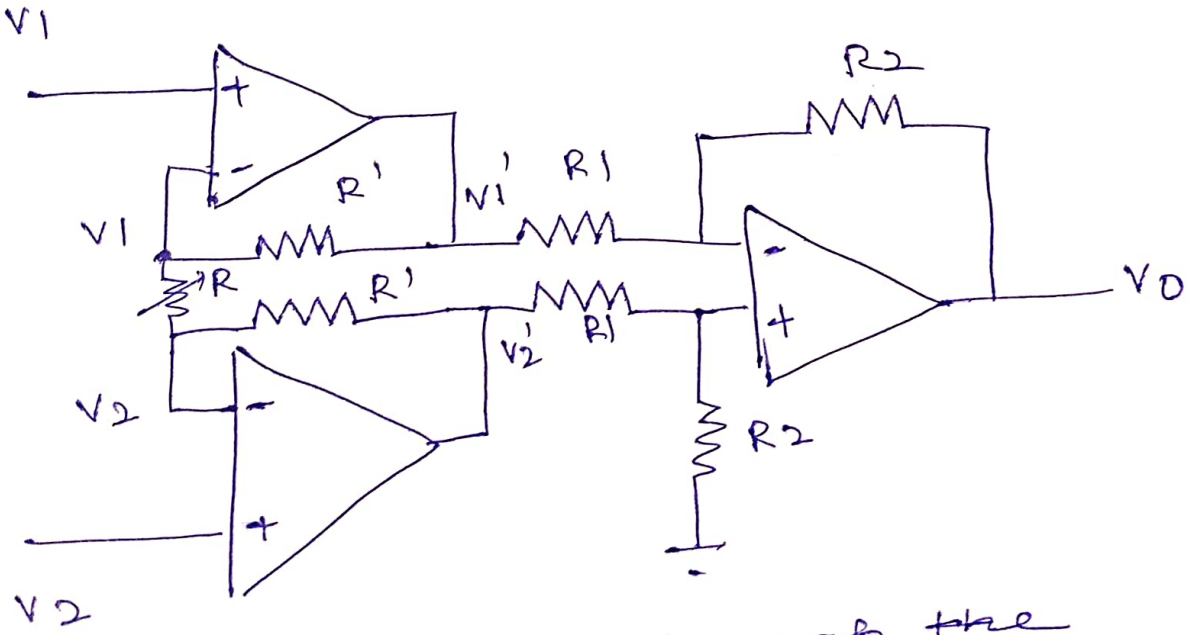
Instrumentation Amplifier

→ used in monitoring and controlling of the physical quantities in the industrial processes for measurement and control of temperature, humidity and light intensity.

→ Transducer which can convert one form energy into another is used to sense and deliver the required information in the form of electrical quantity such as voltage, current or resistance.

Features

- High gain accuracy
- High CMRR
- High gain stability
- Low dc offset
- Low output impedance.



→ current flows through the circuit

$$I = \frac{V_2 - V_1}{R}$$

gain of op-amp A3 is $V_O = \frac{R_2}{R_1}(V_2' - V_1')$

→ current passes through the resistor R_1

$$V_2' = IR' + V_2$$

$$V_2' = \frac{R'}{R}(V_2 - V_1) + V_2$$

$$V_1' = -IR' + V_1$$

$$= -\frac{R'}{R}(V_2 - V_1) + V_1$$

$$V_0 = \frac{R_2}{R_1}\left[\frac{R'}{R}(V_2 - V_1) + V_2 + \frac{R'}{R}(V_2 - V_1) - V_1\right]$$

$$= \frac{R_2}{R_1}(V_2 - V_1)\left[\frac{R'}{R} + \frac{R'}{R} + 1\right]$$

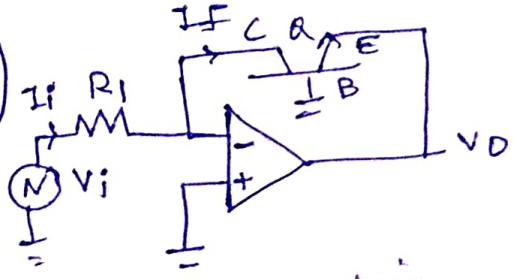
$$\boxed{V_0 = \frac{R_2}{R_1}(V_2 - V_1)\left(1 + \frac{2R'}{R}\right)}$$

Logarithmic Amplifier

→ Logarithmic amplifier called a log amp at logger.

→ basically a current to voltage converter with transfer characteristics

$$V_0 = V_i \ln\left(\frac{I_f}{I_i}\right)$$



→ Transistor Q with its base grounded and its collector at virtual ground is connected in

transdiode configuration.

→ Voltage current relationship

$$I_F = I_S \left[e^{q\frac{V_{BE}}{KT}} - 1 \right]$$

$$I_F = I_C$$

$$I_C = I_S \left[e^{q\frac{V_{BE}}{KT}} - 1 \right]$$

$$\frac{I_C}{I_S} = e^{q\frac{V_{BE}}{KT}} - 1$$

$$e^{q\frac{V_{BE}}{KT}} = 1 + \frac{I_C}{I_S}$$

$$e^{q\frac{V_{BE}}{KT}} = \frac{I_C}{I_S}$$

taking log on both side.

$$\frac{qV_{BE}}{KT} = \ln\left(\frac{I_C}{I_S}\right)$$

$$V_{BE} = \frac{KT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

$$V_{BE} = -V_O \quad , \quad I_i = \frac{V_i}{R_1}$$

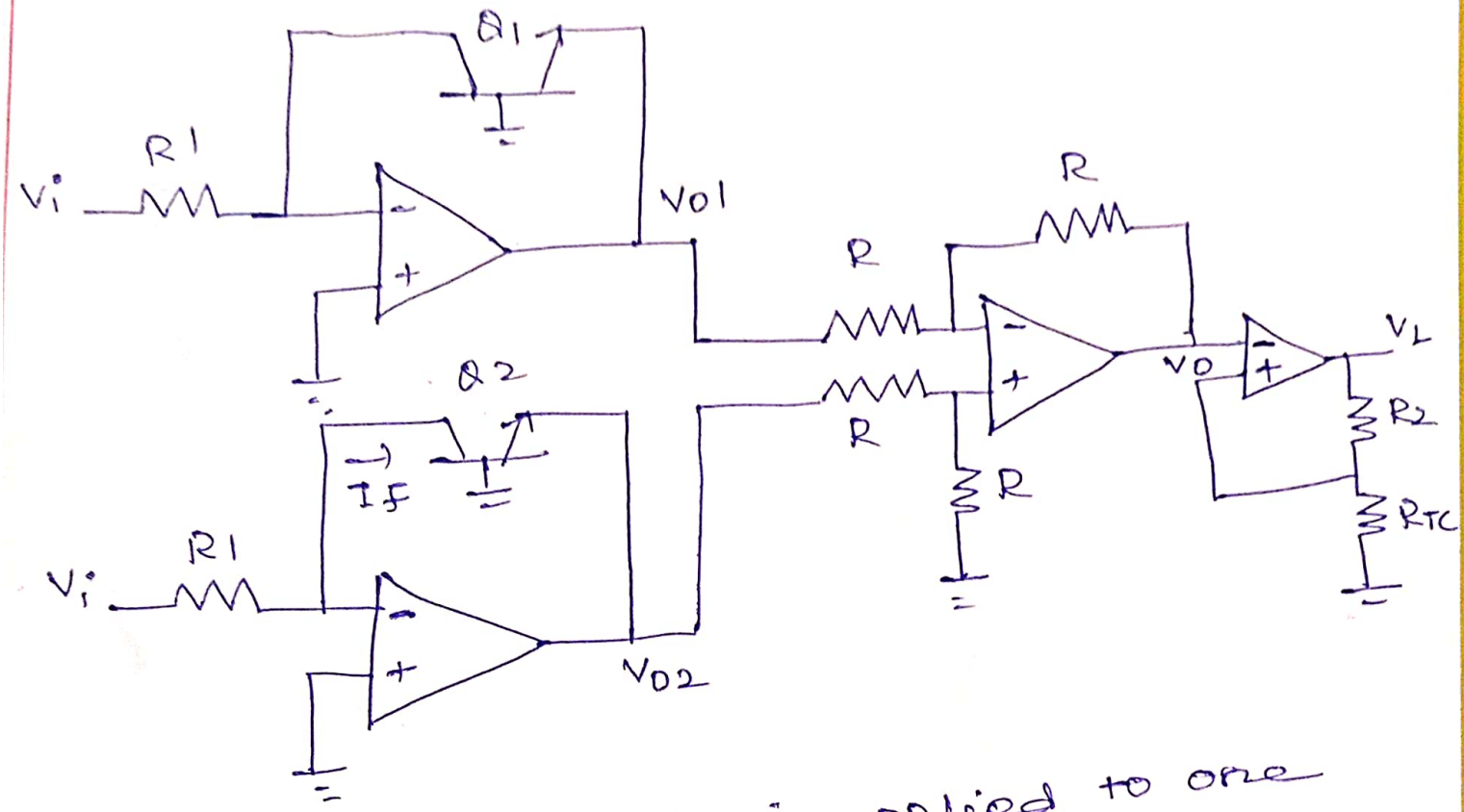
$$V_O = -\frac{KT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

where, $V_R = R_1 I_S$

$$V_O = -\frac{KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$\boxed{V_O = -\frac{KT}{q} \ln\left(\frac{V_i}{V_R}\right)}$$

→ output voltage is rounded to be the logarithmic of input voltage.



→ Input voltage V_i is applied to one log-amp and V_R is applied to another.

$$I_{S1} = I_{S2} = I_S$$

$$V_{O1} = \frac{-KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$V_{O2} = \frac{-KT}{q} \ln\left(\frac{V_R}{R_1 I_S}\right)$$

O/P of A3

$$V_O = V_{O2} - V_{O1} = \frac{-KT}{q} \ln\left(\frac{V_R}{R_1 I_S}\right) + \frac{KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

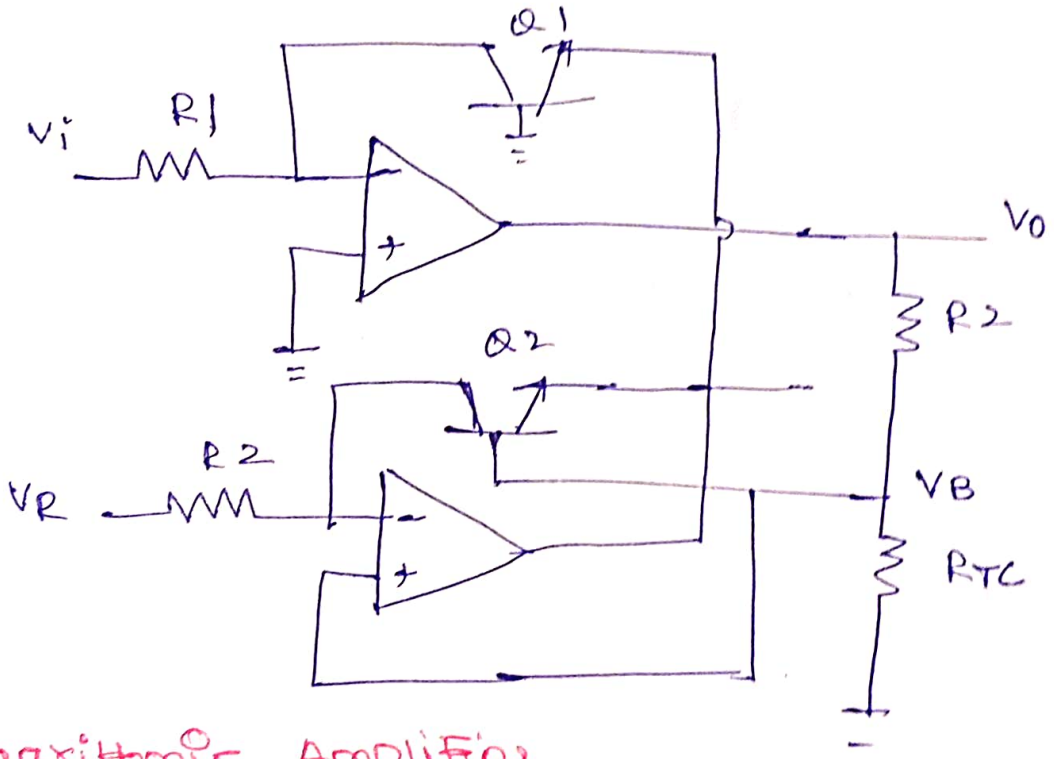
$$= \frac{-KT}{q}\left[\ln\left(\frac{V_R}{R_1 I_S}\right) - \ln\left(\frac{V_i}{R_1 I_S}\right)\right]$$

$$V_o = \frac{KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

op amp A4 acts as compensates for the effects of temperature.

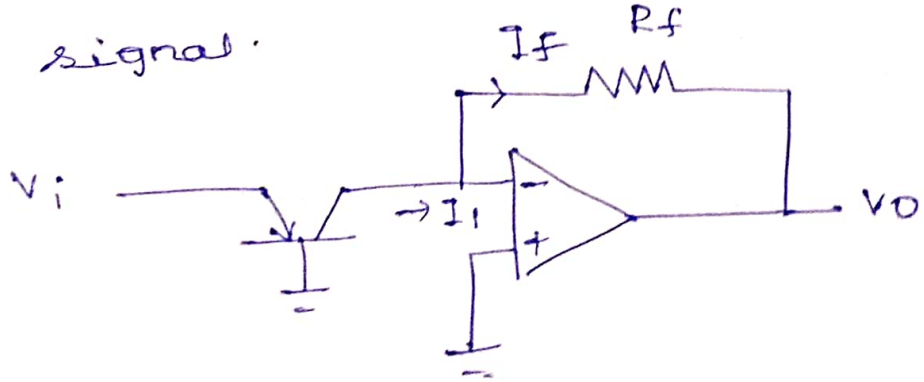
$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right) V_o$$

$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right) - \frac{KT}{q} \ln\left(\frac{V_i}{V_R}\right)$$



Antilogarithmic Amplifier

→ decoding circuit to convert the logarithmically encoded signal back to the real signal.

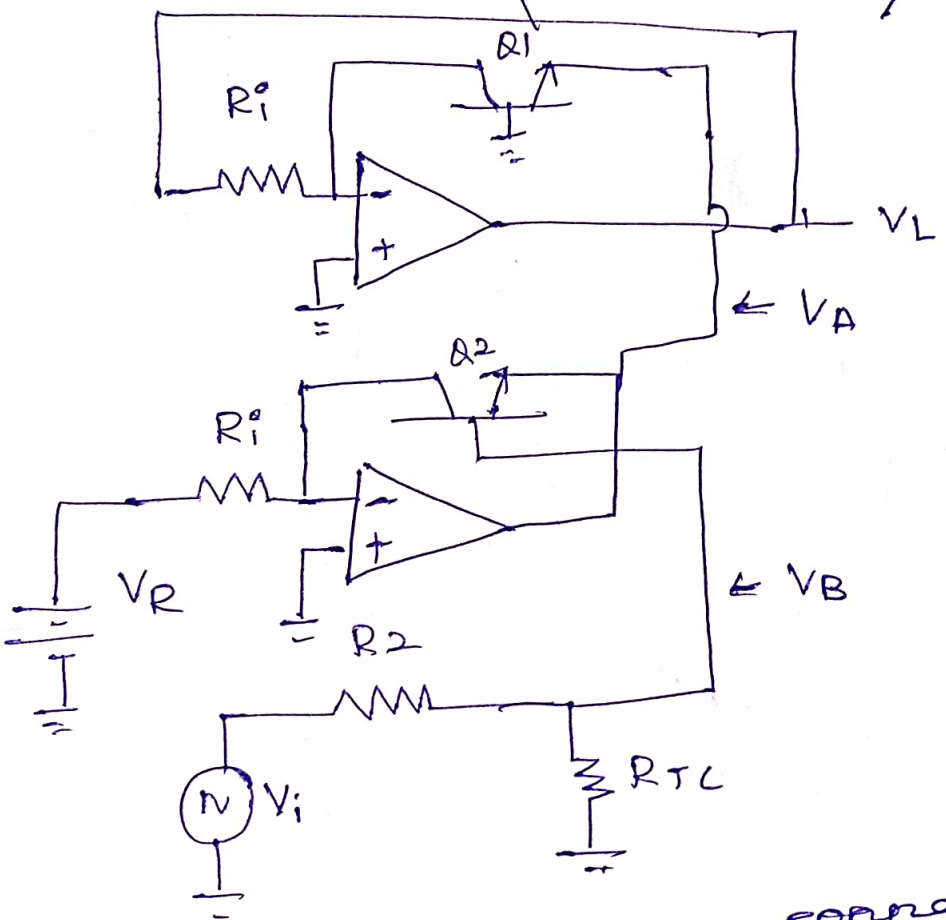


→ Transistor is connected at the inverting input terminal with its base grounded.

→ O/P voltage $V_o = -R_f I_C$

$$I_i = I_C = I_S \left(e^{qV_{BE}/kT} - 1 \right)$$

$$V_o = -R_f I_S \left(e^{qV_{BE}/kT} - 1 \right)$$



Non inverting i/p are connected to ground.

$$V_{BE1} = \frac{kT}{q} \ln \left(\frac{V_L}{R_1 I_3} \right)$$

$$V_{BE2} = \frac{kT}{q} \ln \left(\frac{V_R}{R_1 I_3} \right)$$

$$V_A = -V_{BE1} = -\frac{KT}{q} \ln\left(\frac{V_L}{R_1 I_S}\right)$$

$$V_B = \frac{R_{TC}}{R_2 + R_{TC}} V_i$$

Emitter voltage of Q_2 is

$$V_{2QE} = V_B + V_{BE2}$$

$$V_{Q2E} = \frac{R_{TC}}{R_2 + R_{TC}} V_i + \frac{KT}{q} \ln\left(\frac{V_R}{R_1 I_3}\right)$$

$$V_{Q2E} = V_A$$

$$-\frac{KT}{q} \ln\left(\frac{V_L}{R_1 I_3}\right) = \frac{R_{TC}}{R_2 + R_{TC}} V_i + \frac{KT}{q} \ln\left(\frac{V_R}{R_1 I_3}\right)$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{KT}{q} \ln\left(\frac{V_L}{R_1 I_3}\right) - \frac{KT}{q} \ln\left(\frac{V_R}{R_1 I_3}\right)$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{KT}{q} \ln\left(\frac{V_L}{V_R}\right)$$

$$\ln\left(\frac{V_L}{V_R}\right) = -\frac{q}{KT}\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$\log_{10}\left(\frac{V_L}{V_R}\right) = -0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$\log_{10}\left(\frac{V_L}{V_R}\right) = -K V_i$$

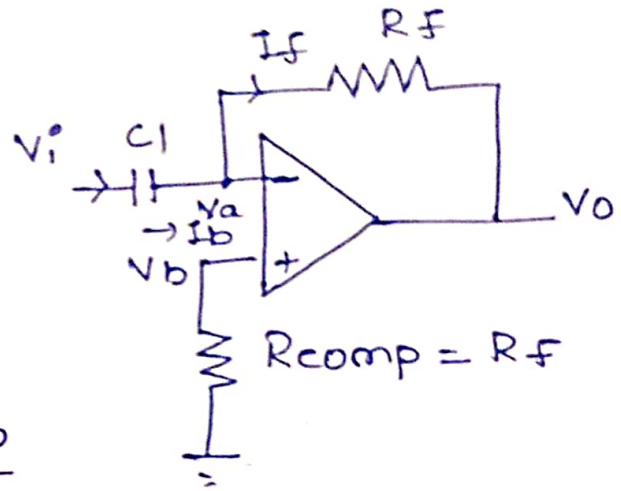
$$K = 0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$\frac{V_L}{V_R} = 10^{-kV_i}$$

$$\boxed{V_L = V_R\, 10^{-kV_i}}$$

Differentiator

→ circuit which produce the differentiation of the input voltage at its output.



KCL,

$$I_1 = I_f + I_b$$

$$I_1 = I_f \qquad I_b = 0$$

$$C_1 \frac{d}{dt} V_{c(f)} = \frac{V_a - V_o}{R_f}$$

$$C_1 \frac{d}{dt}\left[V_i(f) - V_a(f)\right] = -\frac{V_o(f)}{R_f}$$

$$C_1 \frac{d}{dt} V_i(f) = -\frac{V_o(f)}{R_f}$$

$$V_o(f) = -R_f C_1 \frac{d}{dt} V_i(f)$$

Frequency domain

$$V_o(s) = -R_f C_1 s V_i(s)$$

$s = j\omega$

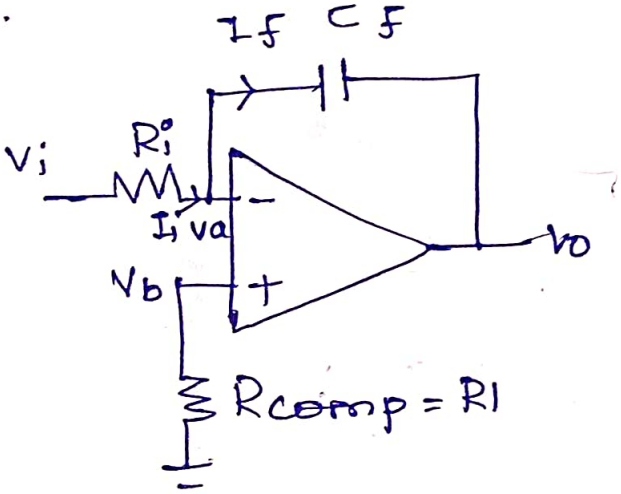
$$V_o(j\omega) = -R_f C_1 j\omega V_i(j\omega)$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega R_f C_1$$

$$|A| = \left| \frac{V_o(jw)}{V_i(jw)} \right| = wR_F C_1$$

Integrator

→ circuit in which the output voltage waveform is the time integral of the input voltage.



KCL,

$$I_i = I_b + I_f$$

$$I_b = 0$$

$$I_i = I_F$$

$$I_F = C\frac{dV_o(t)}{dt}$$

$$= C_F \frac{d}{dt}(V_a - V_o)$$

$$I_i = \frac{V_i - V_a}{R_1}$$

$$\frac{V_i}{R_1} = C_F \frac{d}{dt}(-V_o)$$

Integration on both side

$$\int_0^t \frac{V_i}{R_1} dt = \int_0^t C_F \frac{d}{dt}(-V_o)\, dt$$

$$V_o = -\frac{1}{R_F C_F} \int_0^t V_i(t)\, dt + V_o(0)$$

Frequency domain

$$V_o(s) = -\frac{1}{sR_1C_f} V_i(s)$$

$s = j\omega$

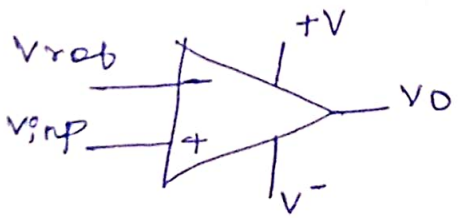
$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_f} V_i(j\omega)$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = +\frac{1}{j\omega R_1 C_f}$$

$$\boxed{|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{1}{\omega R_1 C_f}}$$

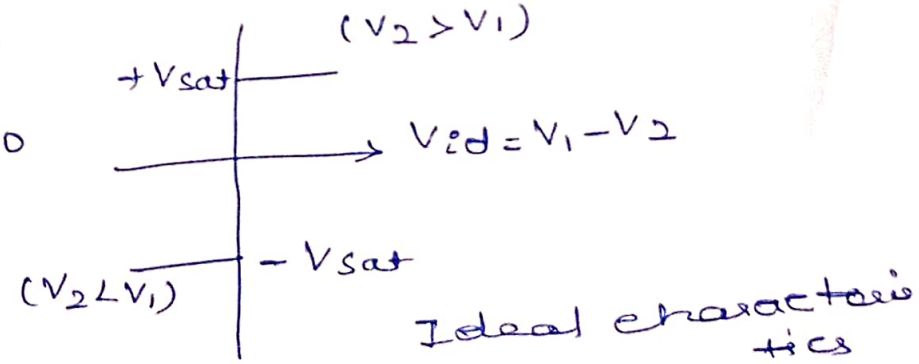
Comparator

→ comparator which compares an input voltage signal with the known voltage

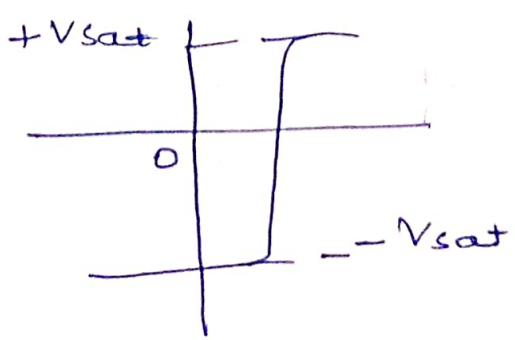


$V_1 = V_{ref}$

$V_2 = V_{inp}$



Ideal characteristics



→ when $V_i < V_{ref}$ then V_{ref} then

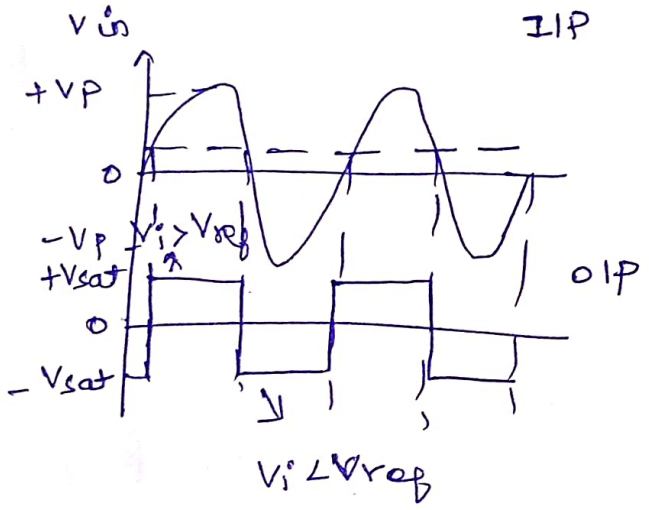
$V_o = V_{sat}$

→ when $V_i > V_{ref}$ then V_{ref} then

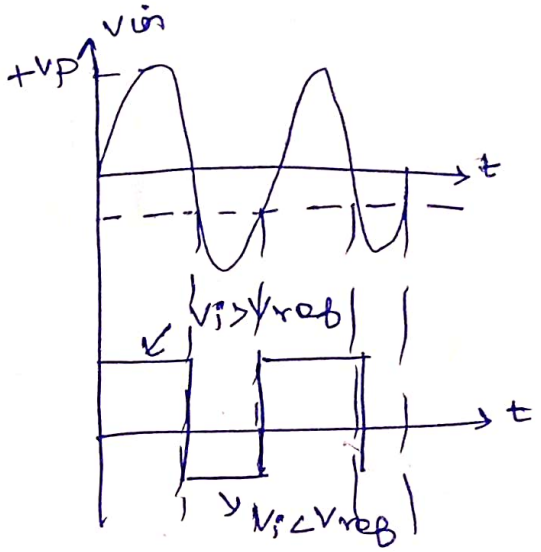
$V_o = -V_{sat}$.

→ $V_i = V_{ref}$ $V_o = 0$

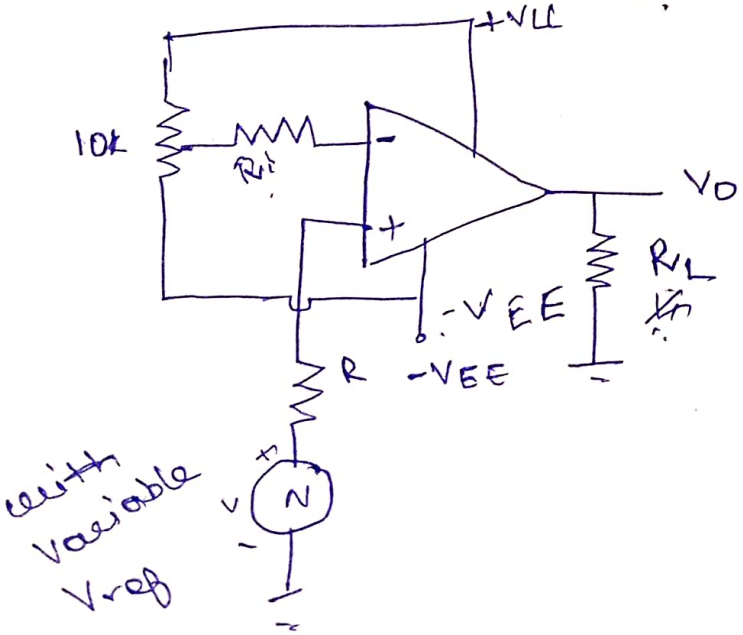
$V_{ref} = +V_e$

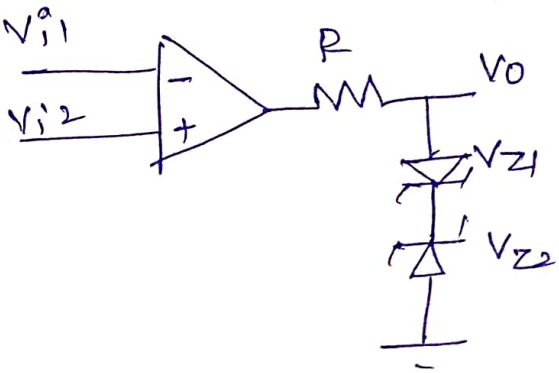


$V_{ref} = -V_e$

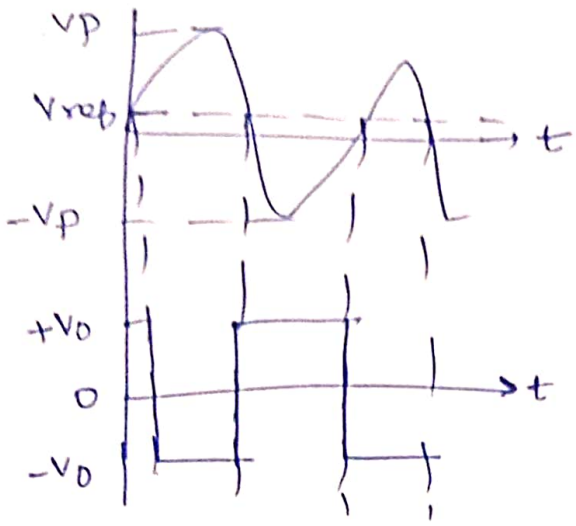


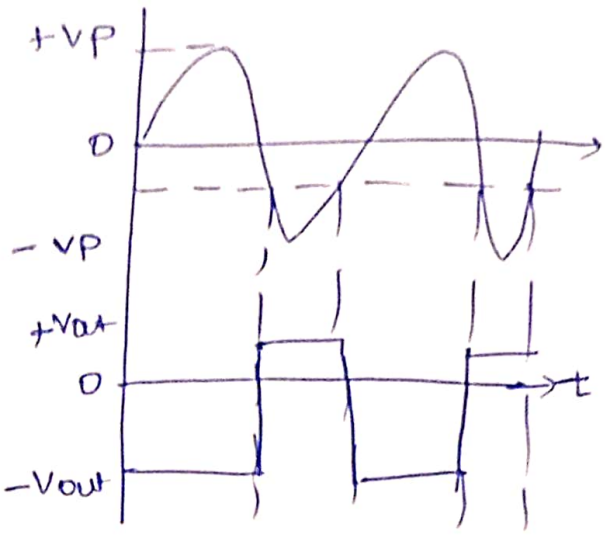
Inverting comparator





with Zener diode at the output.





Application

→ Zero crossing detector

→ Amplitude distribution analyser

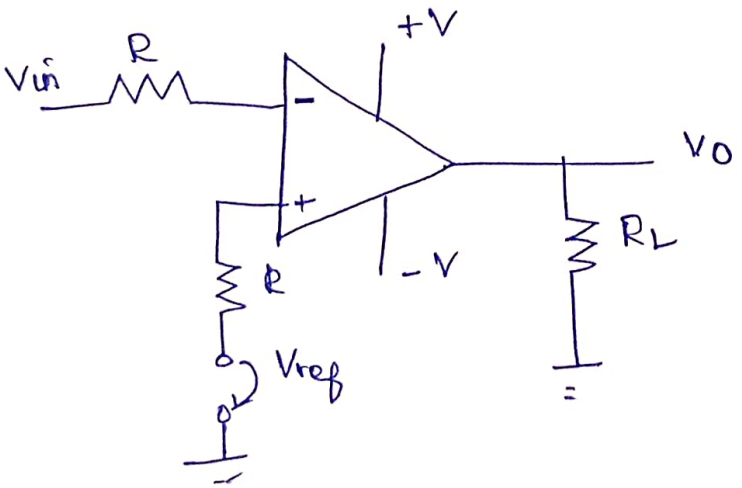
→ pulse time modulator

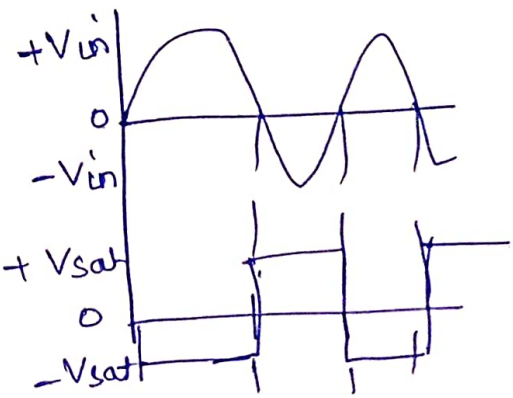
→ window detector

→ time marker generator

→ phase detector.

Zero crossing detector





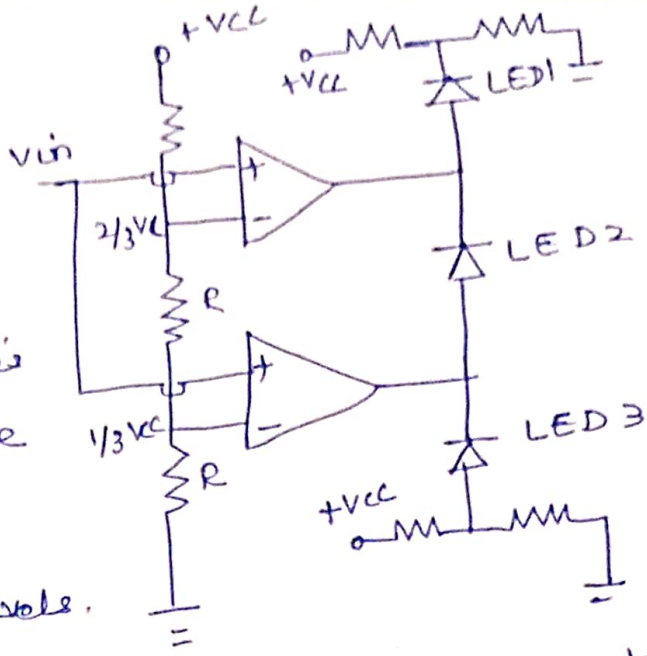
→ The basic comparator is used as zero cross detector with Vref = 0V.

→ Input given as signal but it produce square wave at the output.

Window detector

→ window detector also called a window comparator.

→ used to identifies the unknown voltage falling within two threshold voltage levels.



→ The span of threshold voltage difference is called the window.

→ consider the three level detector with LED indicators. The three LED connected to the output of comparator in series with current limiting resistors.

→ LED will glow when Vi falls within the respective windows.

Input Voltage	LED Glow
Less than 1/3 VCC	LED 3
Between 1/3 VCC & 2/3 VCC	LED 2
Greater than 2/3 VCC	LED 1

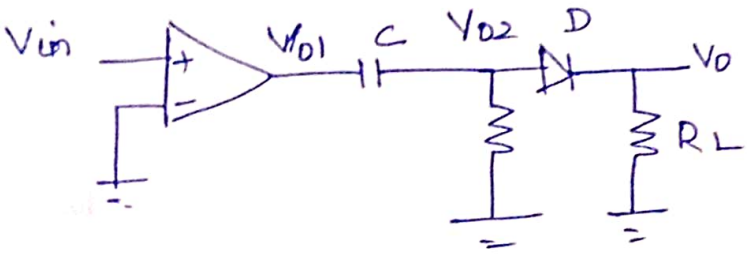
Application

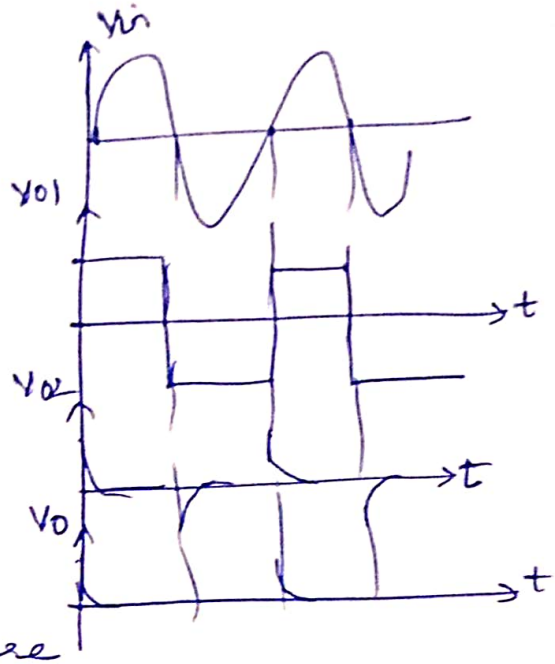
→ production line testing for sorting out defect

→ Raising industrial alarms

→ level detector.

Time marker generator





→ output of zero cross detector circuit is applied to differentiator.

↳ output of the square wave is converted to spike.

→ applied to Half wave rectifier so it produce only positive spikes because D is forward biased.

↳ D is negative — reversed.

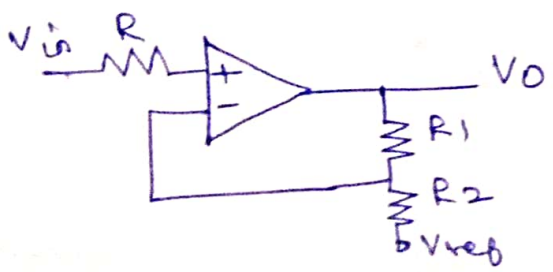
Phase detector

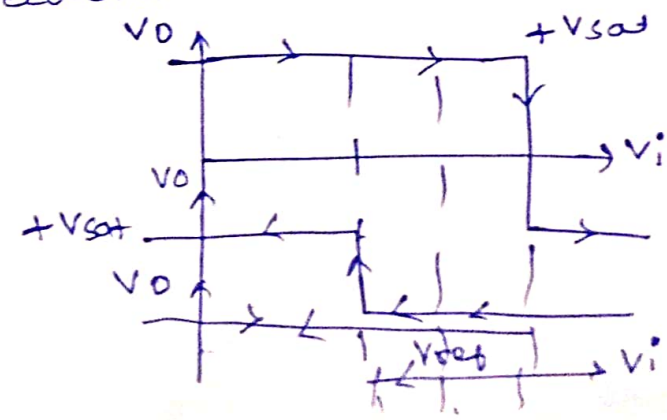
→ phase angle measured.

→ The time interval between the spike.

Schmitt trigger

→ comparator circuit designed with positive feedback to avoid such an unwanted triggering





→ positive feedback makes the gain very large the transfer curve becomes closer to the ideal curve.

→ If loop gain β_{OL} is unity, the gain with feedback A_{Vf} becomes infinite

→ The gain is not maintained as widely for long time because of power supply, temperature variation so the value greater than unity.

→ the difference between the two threshold voltage V_{UT} & V_{LT} is called the hysteresis voltage.

$$V_H = V_{UT} - V_{LT}$$

↳ voltage is at positive saturation with $V_o = +V_{sat}$.

$$V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = V_{UT}$$

↳ V_o remains constant $+V_{sat}$ as long $V_i < V_{UT}$.

↳ V_i just slightly more positive than V_{UT} the output V_o switches from $+V_{sat}$ to $-V_{sat}$

$$V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = V_{LT}$$

$$V_H = V_{UT} - V_{LT}$$

$$= V_{ref} + \frac{R_2}{R_1+R_2}(V_{sat} - V_{ref}) -$$

$$V_{ref} + \frac{R_2}{R_1+R_2}(V_{sat} + V_{ref})$$

$$= V_{ref}\frac{R_1}{R_1+R_2} + V_{sat}\frac{R_2}{R_1+R_2} -$$

$$V_{ref}\frac{R_1}{R_1+R_2} + V_{sat}\frac{R_2}{R_1+R_2}$$

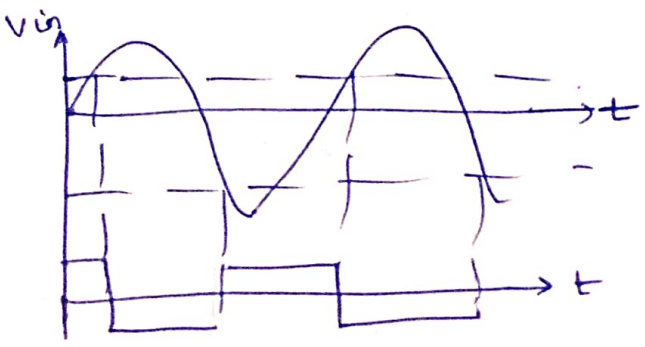
$$= V_{ref}\frac{R_1}{R_1+R_2} + V_{sat}\frac{R_2}{R_1+R_2} -$$

$$V_{ref}\frac{R_1}{R_1+R_2} + V_{sat}\frac{R_2}{R_1+R_2}$$

$$R_3 = R_1 \| R_2$$

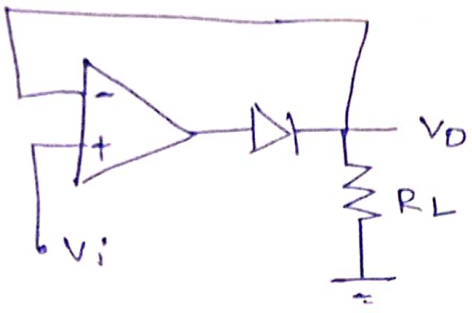
$$\boxed{V_{UT} = -V_{LT} = \frac{R_2}{R_1+R_2} V_{sat}}$$

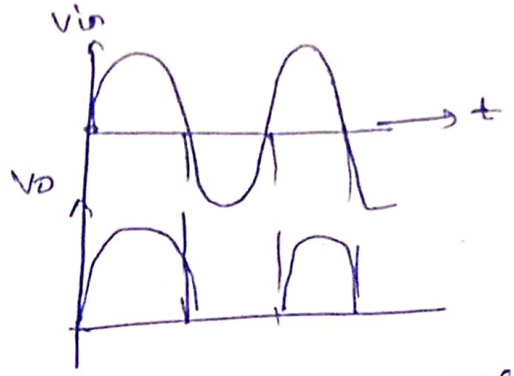
→ To convert very slowly varying input voltage into a square wave output



Precision Rectifier

→ major limitations of ordinary diode is that it cannot rectify voltage below the cut in voltage of the diode.





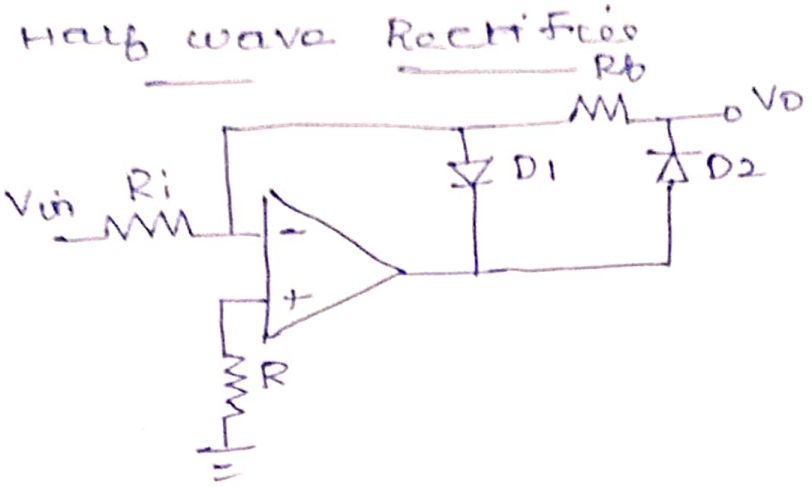
→ If $V_i = +V_e$ op amp output also positive then the closed loop condition is achieved for op-amp, $V_o - V_i$

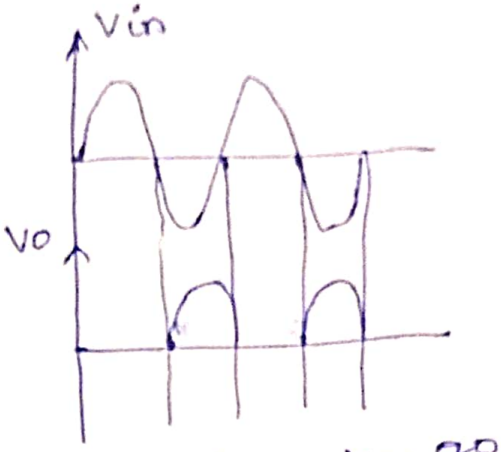
→ If $V_i < 0$, $-V_e$ the op-amp for output is negative and the diode D is reverse biased

→ $V_o = 0$, D if off and no current is delivered to the load R_L except for small bias current of non amp and the reverse saturation current of diode

Application
- → Half wave rectifier
- → Full wave rectifier
- → peak detector
- → clipper
- → clamper.

Half wave Rectifier





→ $V_i > 0$ (+ve) D_1 conducts causing V_{o1} go to negative by one diode drops

↳ D_2 is reverse biased

→ output voltage is zero because no current flow through R_f and the input current flow through D_1.

→ $V_i < 0$ (-ve) D_2 conducts and D_1 is off

↳ negative input forces the op-amp.

↳ V_{o1} is positive causes D_2 to conduct the circuit then acts like an inverter

For $R_f = R_1$ & $V_o = +V_a$ circuit.

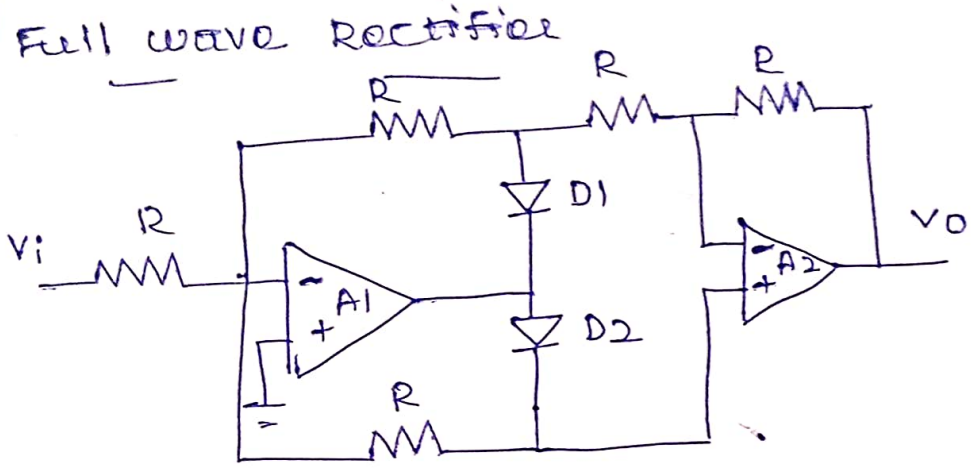
$V_o = 0$ when $V_i = 0$

$$V_o = -\frac{R_f}{R_i} \quad V_i < 0$$

$V_{o1} = -0.6$ for $V_i > 0V$

$$V_{o1} = \frac{R_f}{R_1} V_i + 0.6V \text{ for } V_i < 0V.$$

Full wave Rectifier



→ positive voltage $V_i > 0$.

D_1 = on

D_2 = off

Both op amp acts as inverter

$$V_o = V_i$$

→ negative voltage $V_i < 0$

D_1 - off

D_2 - ON

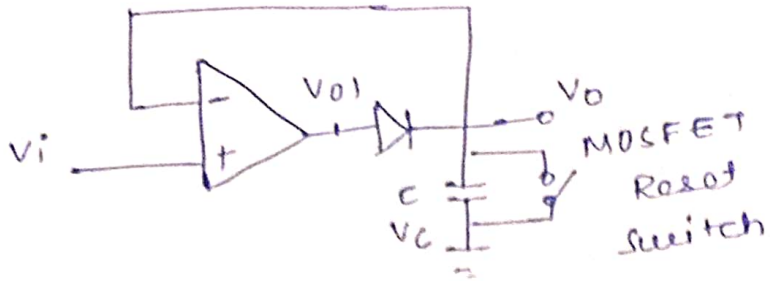
Output of A1 is inverter o/p and differential input to A2 is zero so $V_o = V_i$

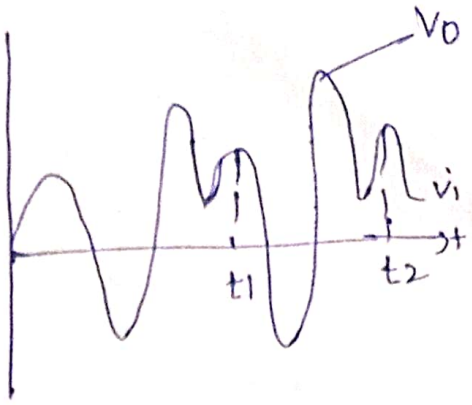
$$V_o = V_i$$

Peak Detector

→ produces an output voltage equal to the positive or negative peak value of the input voltage.

→ function of a peak detector is compute the peak value of signal input.





→ Highest peak value is stored until the capacitor is discharged.

operation

→ Vi > Vc, D is forward biased and the circuit becomes voltage follower. So the output voltage Vo follow Vi

→ Vi drops below Vc is Vi > Vc D is reverse biased and the capacitor holds the charge till input voltage again attains the value > Vc.

→ peak at time t_1 and t_2 is missed because of the above reason.

→ circuit can be reset the capacitor voltage can be made zero by Connecting Switch across capacitor,

→ To holds the lowest or negative Voltage peak signal the diode D is connected as reverse direction.

Clipper

→ called amplitude limiter

→ used to clip off portion of the input signal.

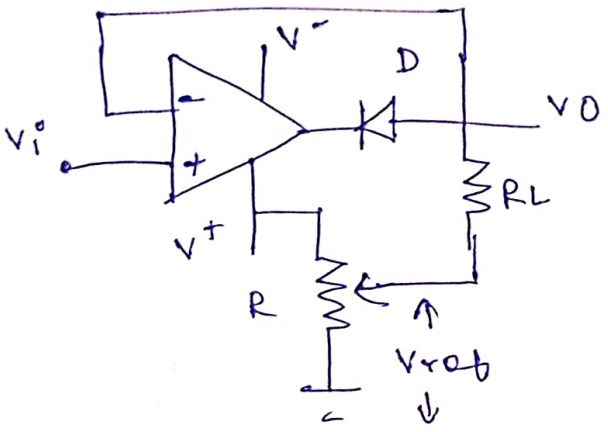
Types

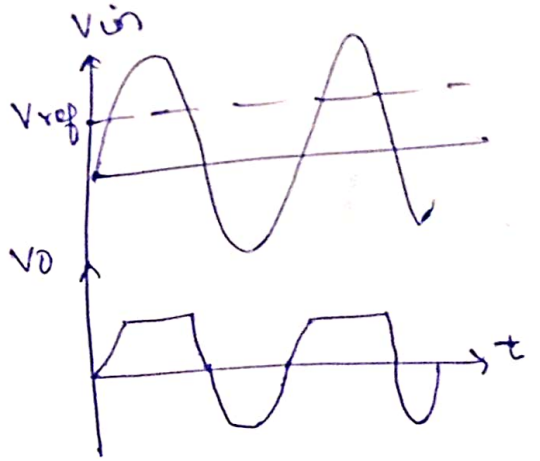
↳ positive clipper

↳ negative clipper.

positive clipper

→ clip the positive position





→ clipping level is determined by the reference voltage Vref

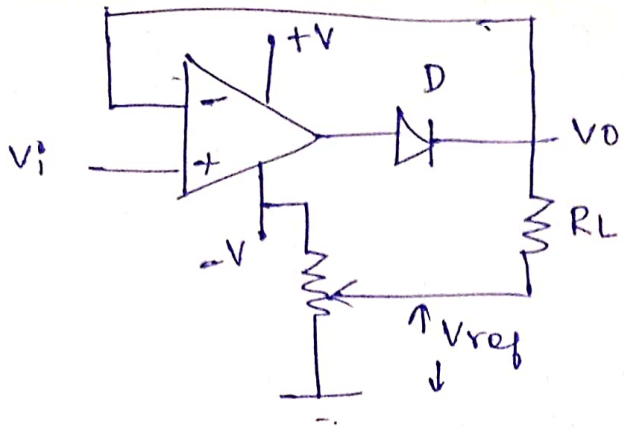
↳ $V_i < V_{ref}$ D = conduct, opamp work as voltage follower.

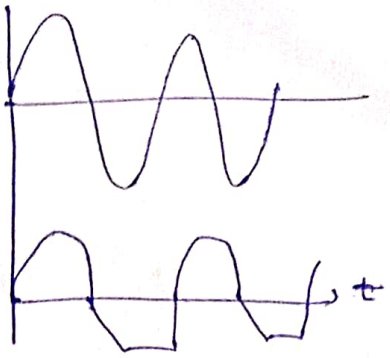
↳ $V_i \leq V_{ref}$ D = cutoff so $V_o < V_{ref}$

↳ $V_{ref} = -V_e$ the entire portion above Vref is clipped off.

Negative clipper

→ clips the negative position.





→ negative clipper cut off the position below the Vref.

clamper

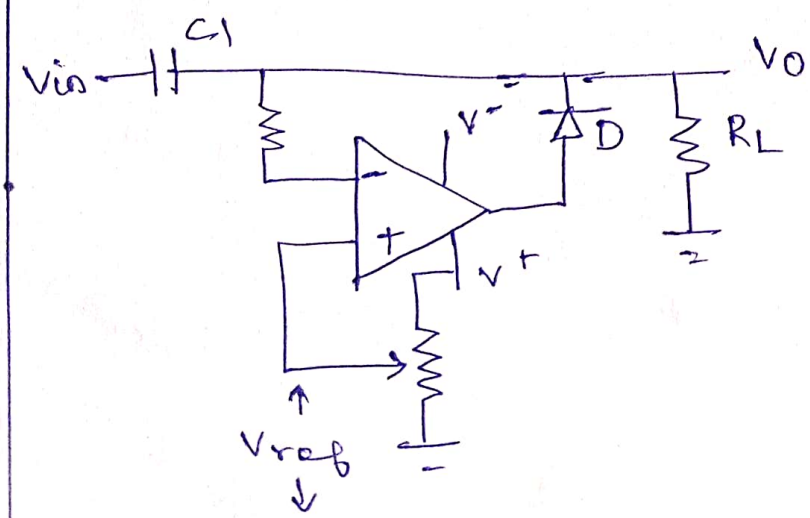
→ dc inverter

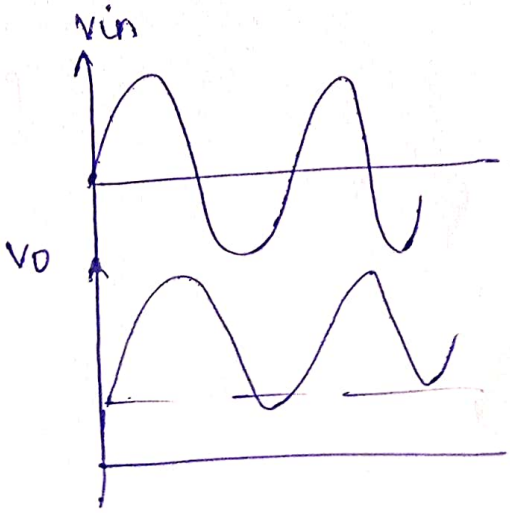
→ output is clamped to a desired dc level.

→ clamped dc level is positive it is called positive clamper.

→ If the clamped level is negative it is called negative clamper.

positive clamper





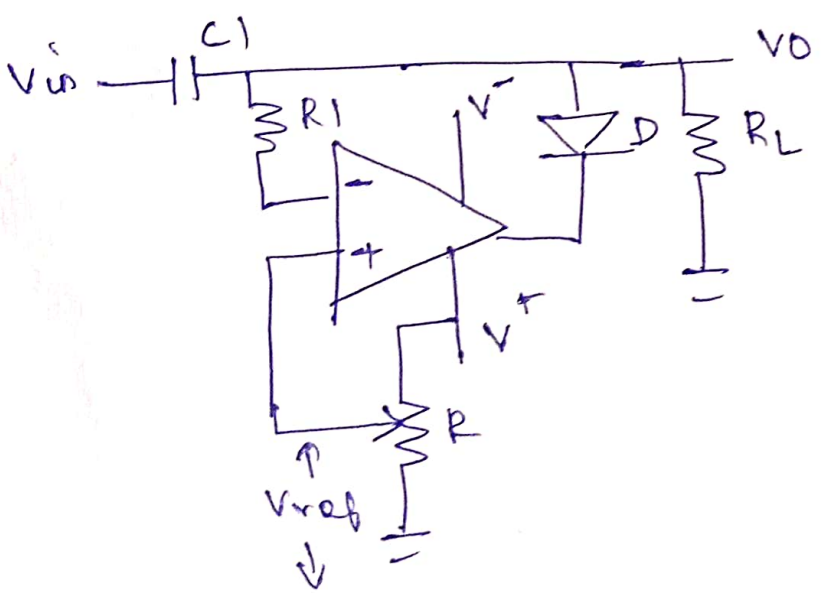
→ Vref applied to +ve input terminal.
For positive Vref the D is forward biased.
The op-amp operates as voltage follower
So $\boxed{V_O = +V_{ref}}$

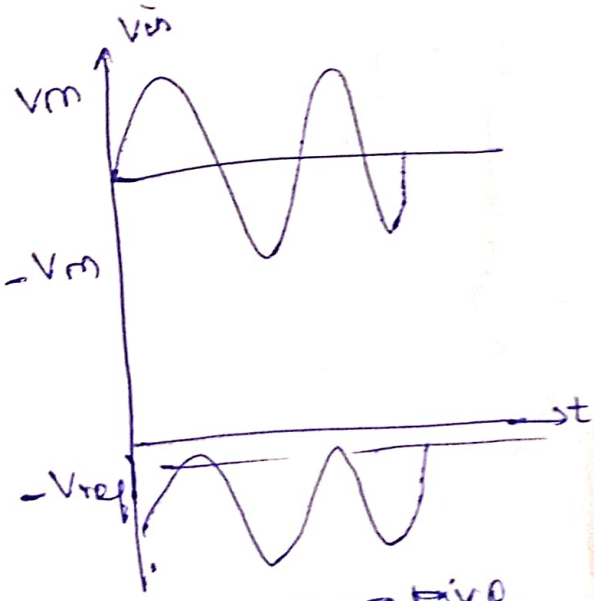
→ $V_i = V_m \sin \omega t$ at applied at -ve terminal during -ve half cycle of V_i

↳ D conducts the capacitor C1 charges through D to $-V_m$ during +ve half cycle of V_i, D is reverse biased the capacitor retains the previous voltage V_m

$$\boxed{V_O = V_{ref} + V_i + V_m}$$

Negative clamper





→ By reversing the diode D, negative clamper is constructed.

→ The resistor R_1 is used for protecting op-amp against excessive discharge from C_1 when dc supply voltage switched off.

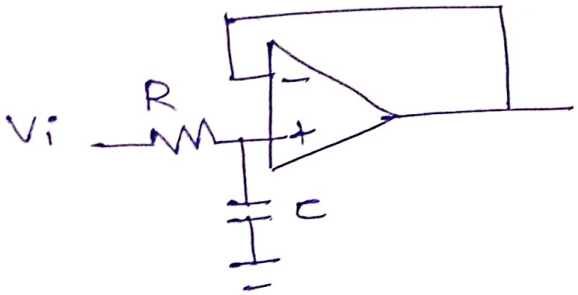
Filters

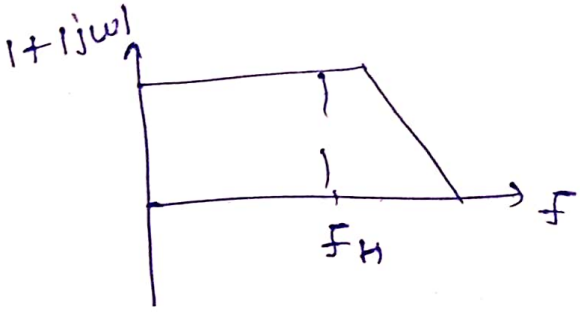
→ designed to pass a specified band of frequencies.

LPF, HPF, BPF, BSF

LPF

→ only low frequency signals upto certain breakpoint f_L.





transfer characteristics

$$H(S) = \frac{V_o(S)}{V_i(S)}$$

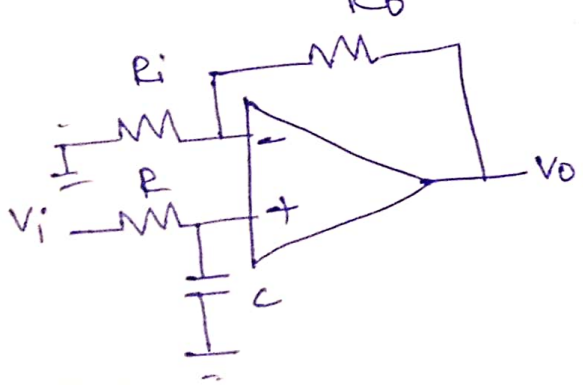
$$= \frac{1/SC}{R+1/SC} = \frac{1}{1+SCR}$$

$$H(j\omega) = \frac{1}{1+j\frac{\omega}{\omega_H}}$$

$$\omega_H = 1/RC$$

$$|H(j\omega)| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_H}\right)^2}}$$

with variable Gain



$$X_C = \frac{1}{2\pi fC}$$

$$V_1 = \frac{-jX_C}{R-jX_C} V_{in}$$

$$= \frac{-j\left(\frac{1}{2\pi f_c}\right)}{R - j\left(\frac{1}{2\pi f_c}\right)} V_{in}$$

$$V_1 = \frac{-j}{2\pi f R_c - j} V_{in}$$

Op-amp is in non inverting amplifier

$$V_O = \left(1 + \frac{R_f}{R_i}\right) V_i$$

$$= \left(1 + \frac{R_f}{R_i}\right) \frac{-j}{2\pi f R_c - j} V_{in}$$

$$\frac{V_O}{V_{in}} = \frac{A_F}{1 + j(f/f_H)}$$

$$\text{Gain} = \left|\frac{V_O}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

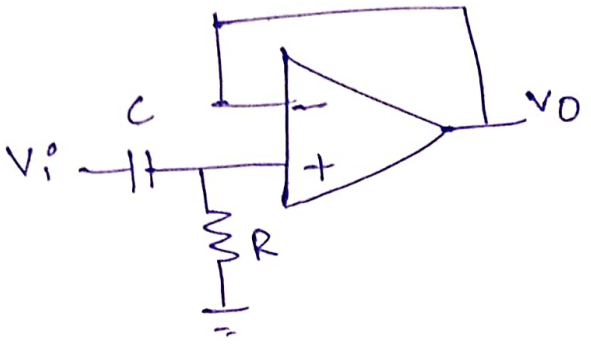
$f < f_H$, $\left|\frac{V_O}{V_{in}}\right| \simeq A_F$ is constant

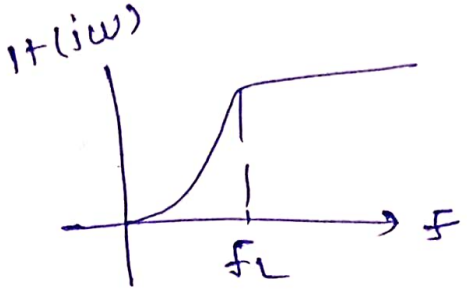
$f = f_H$, $\left|\frac{V_O}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\, A_F$

$f > f_H$, $\left|\frac{V_O}{V_{in}}\right| < A_F$

HPF

→ allows only frequencies above a certain break point f_H, and attenuates the low frequency components

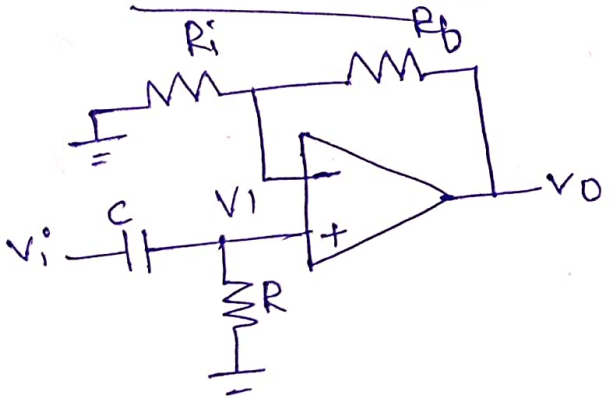


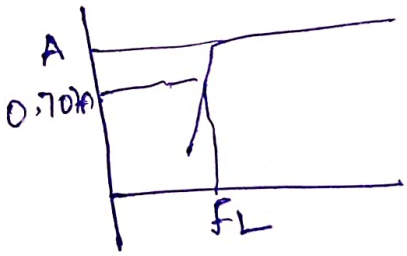


Transfer function

$$H(S) = \frac{V_o(S)}{V_i(S)} = \frac{R}{R+1/SC} = \frac{1}{1+1/SRC}$$

with variable gain





→ At high frequencies, the capacitor appears shorted gain = $1 + \frac{R_f}{R_i}$

$$V_o = \left(1+\frac{R_f}{R_i}\right)\left(\frac{j2\pi fRC}{1+j2\pi fRC}\right)V_i$$

$$\frac{V_o}{V_i} = \left(1+\frac{R_f}{R_i}\right)\left(\frac{j2\pi fRC}{1+j2\pi fRC}\right)$$

$$\boxed{\frac{V_o}{V_i} = A\ \frac{jf/f_L}{1+j(f/f_L)}}$$

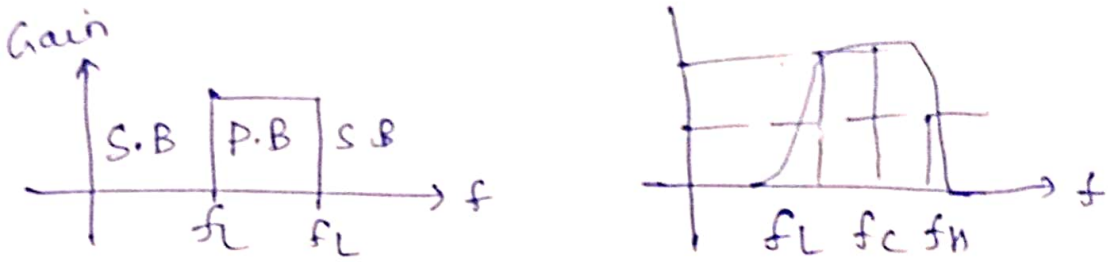
$$f_L = 1/2\pi RC$$

$$|1-(j\omega)| = \left|\frac{V_O}{V_i}\right| = \frac{A}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}$$

BPF

→ combination of LPF and HPF.

→ It allows the frequency between F_L and F_H



$$\boxed{B = f_H - f_L}$$

→ Frequency

$$f_r = \sqrt{f_L f_H}$$

→ figure of merit

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{B}$$

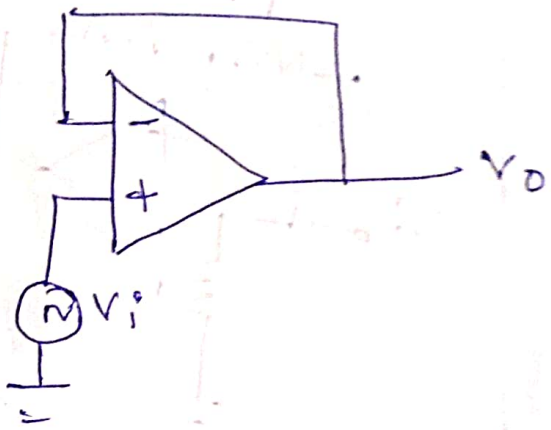
Two types

→ Narrow band pass filter

→ wide band pass filter.

Voltage follower

$R_1 = \infty$, $R_f = 0$.



→ The amplifier acts as unity gain amplifier

→ In Non Inverting amplifier, V_o

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

$$V_o = \left(1 + \frac{0}{\infty}\right) V_1$$

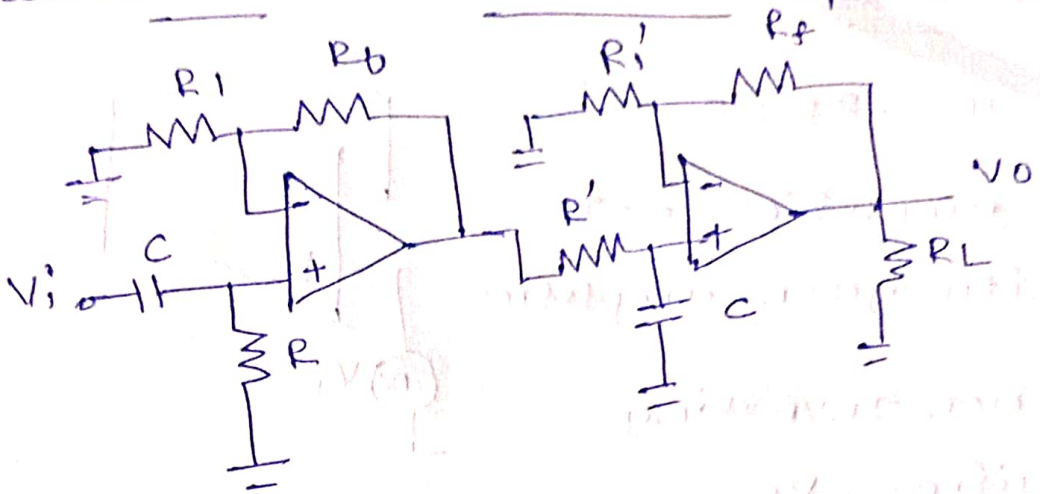
$$= (1 + 0)\, V_1$$

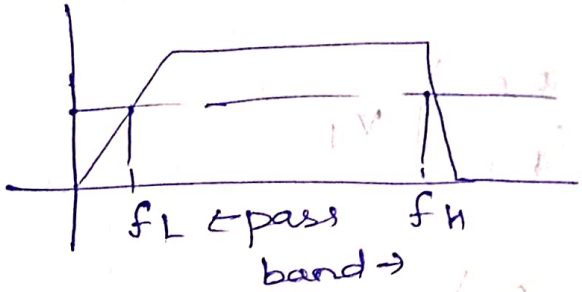
$$\boxed{V_o = V_1}$$

→ The output voltage is equal to the input voltage both in magnitude and phase.

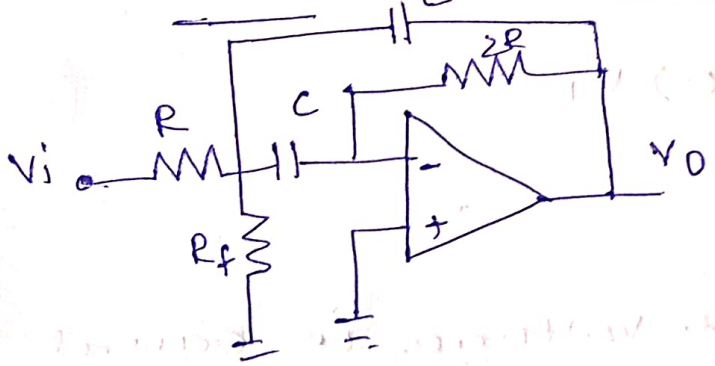
→ The output voltage of the circuit follows the input voltage.

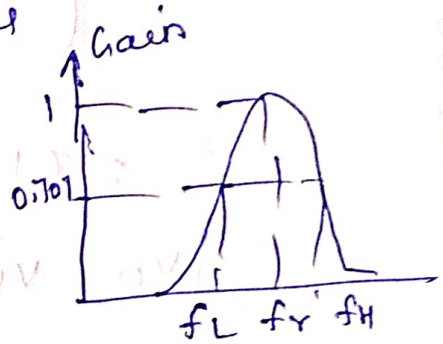
wide band pass filter





Narrow band pass filter





→ band pass is very narrow and the bandwidth is very small.

$$B = \frac{0.1591}{RC}$$

$$B = f_r / Q.$$

$$f_r = \frac{0.1125}{RC}\sqrt{1 + \frac{R}{R_r}}.$$

—x— x —

Unit-3

Timer circuits, VCO and PLL

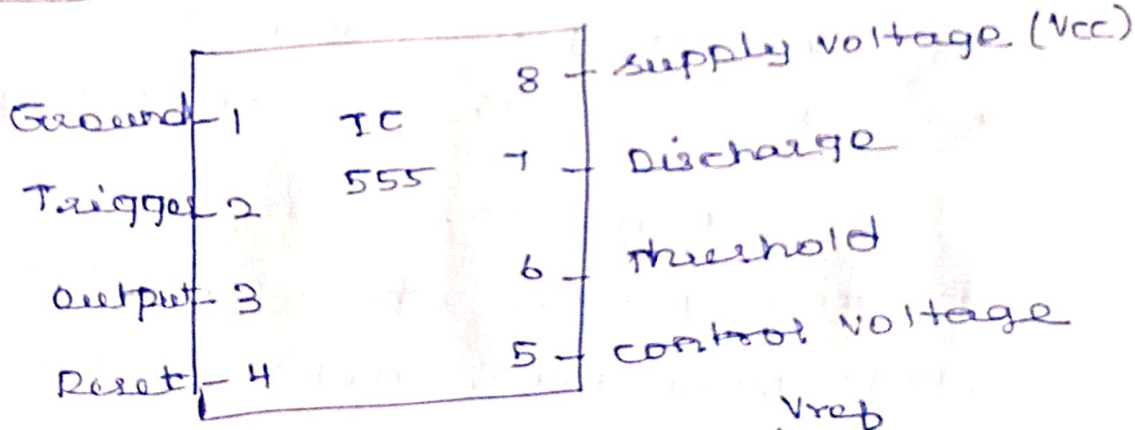
IC 555 Timer

→ Timer IC 555 is most versatile linear integrated device.

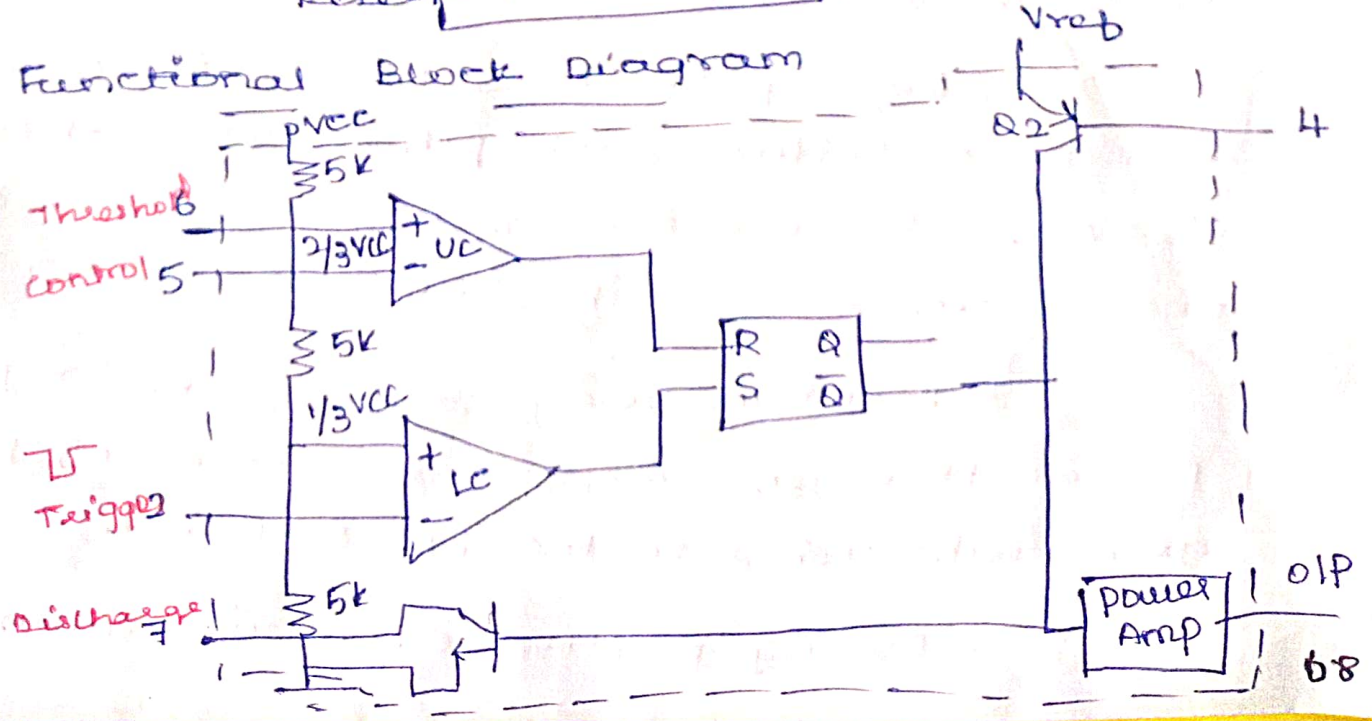
→ basically a monolithic timer circuit which can be used in many applications such as

- Monostable multivibrator
- Astable multivibrator
- Linear ramp generator
- missing pulse generator.

pin Diagram



Functional Block Diagram



→ Three 5k internal resistors act as voltage divider, providing bias voltage of 2/3 Vcc to upper comparator (UC) & 1/3 Vcc to lower comparator (LC)

→ Two voltages fix the necessary comparator threshold voltage.

↳ standby (stable) state the output $\bar{Q}$ of FF is High.

↳ the output Q Low because of power amplifier which is basically an inverter.

↳ negative going trigger pulse is applied to pin 2 and its dc level greater than threshold level of LC is Vcc/3.

↳ negative going edge of the trigger, passes through (Vcc/3) the output of LC goes high and sets the FF ($Q=1, \bar{Q}=0$)

↳ During positive excursion when the threshold voltage at pin 6 passes through (2/3 Vcc), the output of upper comparator goes high resets the FF ($Q=1, \bar{Q}=0$)

↳ negative going edge of the trigger, passes through (Vcc/3) the output of LC goes high and sets the FF ($Q=1, \bar{Q}=0$)

↳ During positive excursion when the

threshold voltage at pin 6 passes through (2/3 Vcc), the output of upper comparator goes high resets the FF ($Q=1, \bar{Q}=0$)

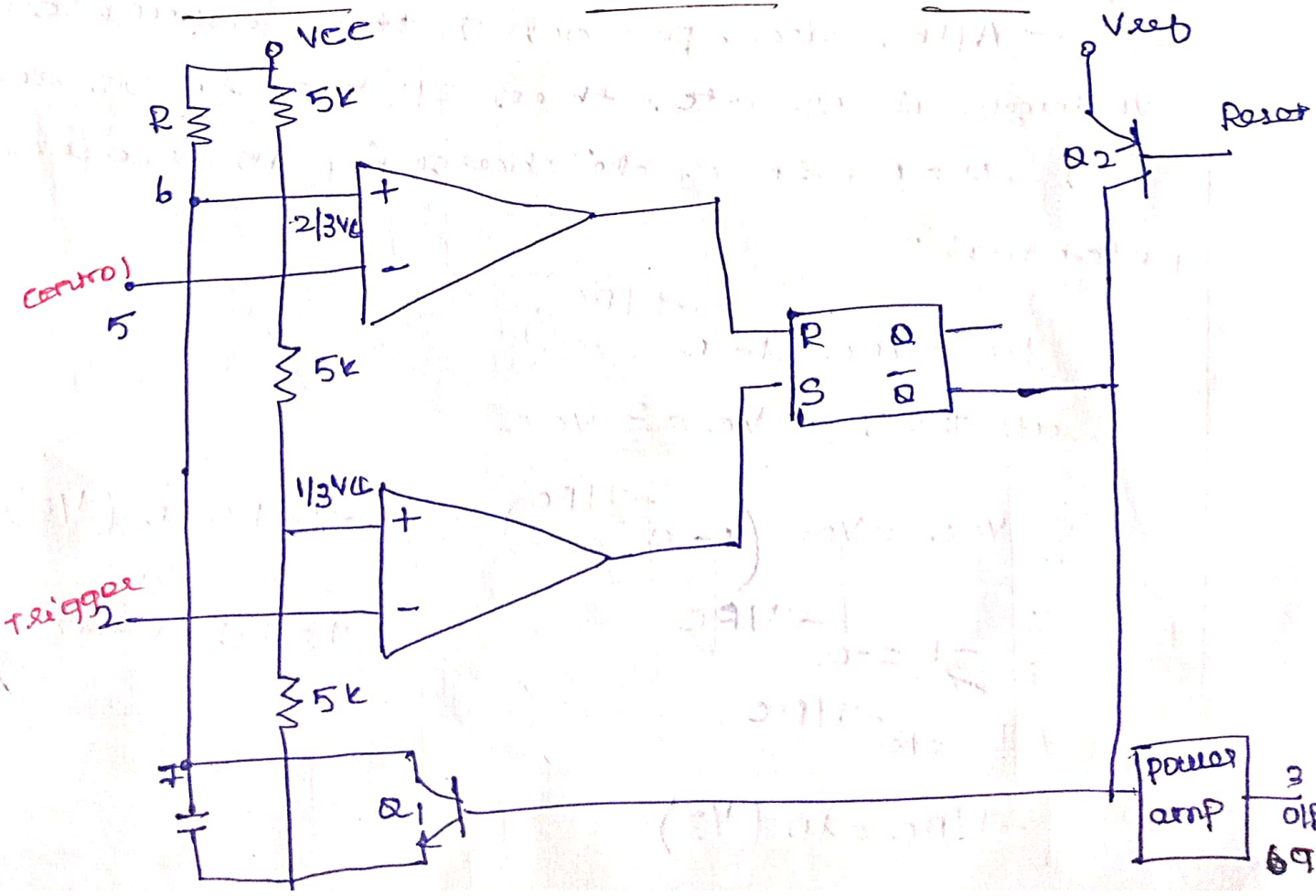
→ Reset input provides a mechanism to reset the FF. This overriding reset is effective when reset is less than about 0.4V

→ Reset is not used, it is returned to Vcc

→ Transistor Q_2 serves as buffer to isolate the reset from FF and Q_1.

→ Q_2 is driven by the internal reference voltage V_{ref} obtained from Vcc.

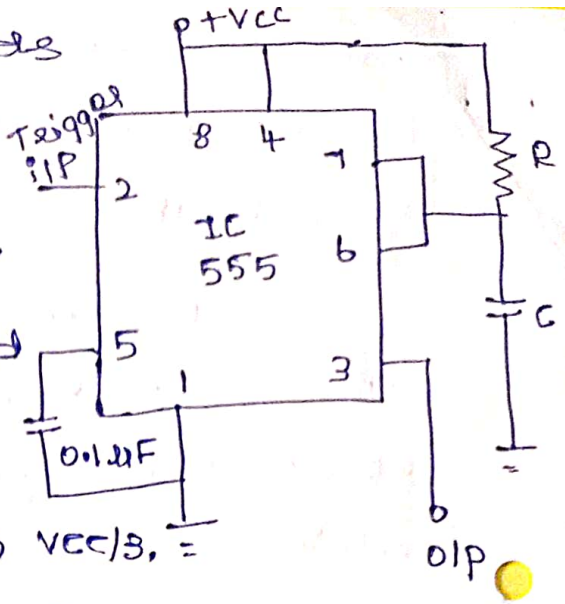
Monostable multivibrator using IC 555



→ In stable state, FF holds transistor Q1 - ON

↳ the external Timing capacitor C to Gnd.

↳ O/p remains at ground potential is low



→ Trigger passes through Vcc/3, =

↳ FF is set is Q=0

↳ Q1 OFF and short circuit across the timing capacitor C is released.

→ transistor is low, the output goes High the timing cycle now begins since voltage across C rises through R towards Vcc with time constant RC.

→ After time period of the capacitor voltage is greater than 2/3 Vcc so Vc reaches & $\bar{Q}=1$, $Q=0$, so C discharging to ground potential.

$$V_c = V_{cc}\left(1-e^{-t/RC}\right)$$

at $t=T$, $V_c = \frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}\left(1-e^{-T/RC}\right)$$

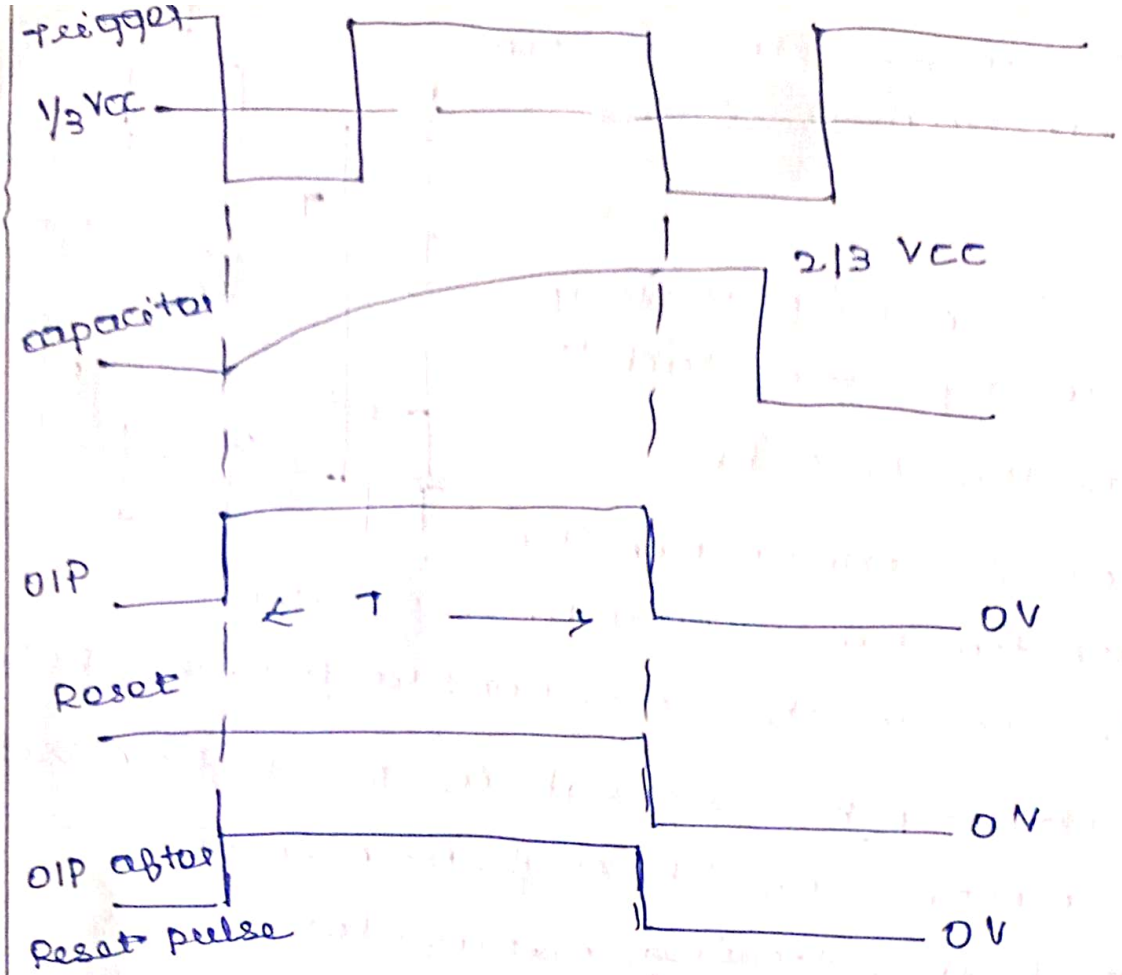
$$\frac{2}{3}-1 = -e^{-T/RC}$$

$$+\frac{1}{3} = +e^{-T/RC}$$

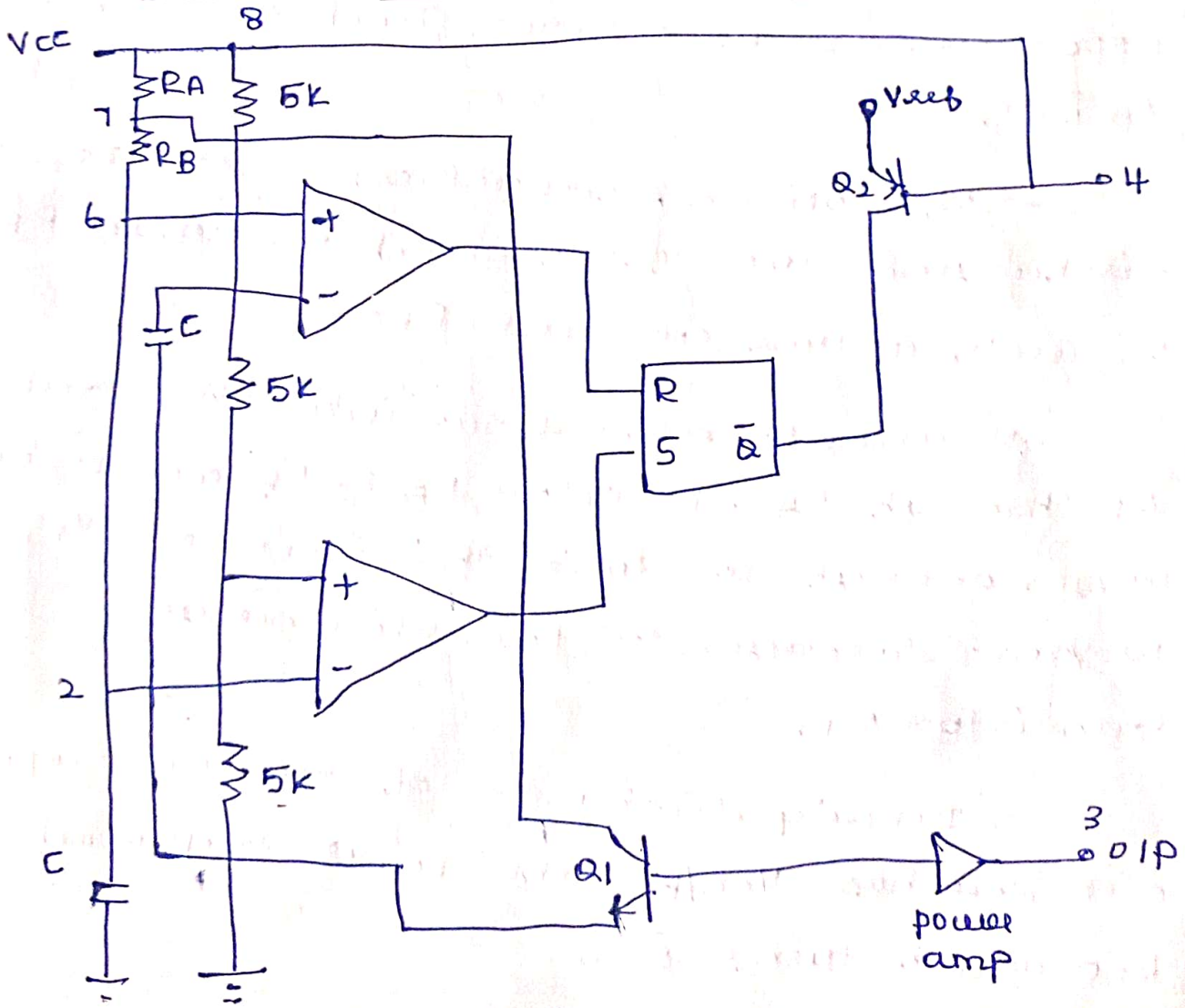
$$-T/RC = \ln(1/3)$$

$$-T = RC \ln(1/3)$$

$$T = 1.1\ RC \text{ sec}$$

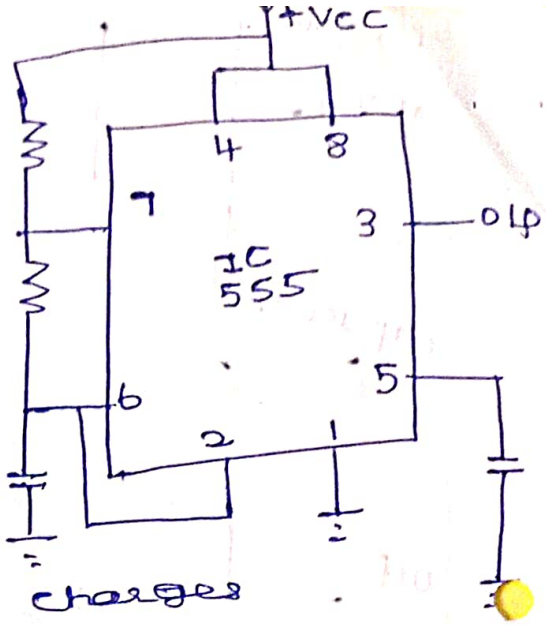


Astable multivibrator using IC 555



→ Timing resistor is now split into two resistors R_A & R_B

→ Pin 7 of discharging transistor Q_1 connected to the junction R_A & R_B



→ Vcc is connected, the external timing capacitor C charges towards Vcc with time constant $(R_A + R_B)C$

→ output pin 3 is high as Reset R=0 & set S=1.

→ so the output of FF Q=1, $\bar{Q}=0$, which unclamped the timing capacitor C.

→ capacitor voltage equals 2/3 Vcc, the upper comparator triggers and control flipflop so $\bar{Q}=1$.

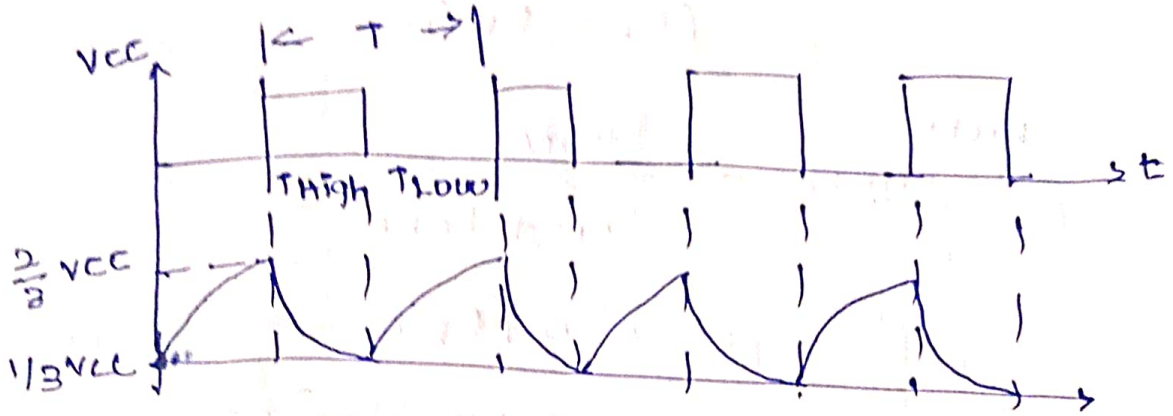
→ Q_1 - ON and capacitor C starts discharging towards ground through R_B and Q_1 with a time constant R_BC.

→ current also flows into the transistor Q_1 through R_A. Resistor R_A & R_B must be large enough to limit this current & prevent damage to the discharge transistor Q_1.

→ During discharge of timing capacitor C it reaches Vcc/3, the IC is triggered S=1, R=0 which turns $\bar{Q}=0$.

→ capacitor is charged and discharged between 2/3 Vcc and 1/3 Vcc

$$V_c = V_{cc}\left(1 - e^{-t1/RC}\right)$$



t_1 taken by the circuit to charge from 0 to 2/3 Vcc is

$$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-t1/RC}\right)$$

$$t_1 = 1.09\,RC$$

t_2 taken by the circuit to charge from 0 to 1/3 Vcc

$$\frac{1}{3}V_{cc} = V_{cc}\left(1 - e^{-t1/RC}\right)$$

$$t_2 = 0.405\,RC$$

Time to charge from 1/3 Vcc to 2/3 Vcc

$$t_{High} = t_1 - t_2$$

$$= 1.09RC - 0.405RC$$

$$t_{High} = 0.69RC$$

$$T = t_{high} + T_{low}$$

$$= 0.69\,(R_A + 2R_B)C$$

$$F = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C}$$

$$= \frac{1.45}{(R_A + R_B)C}$$

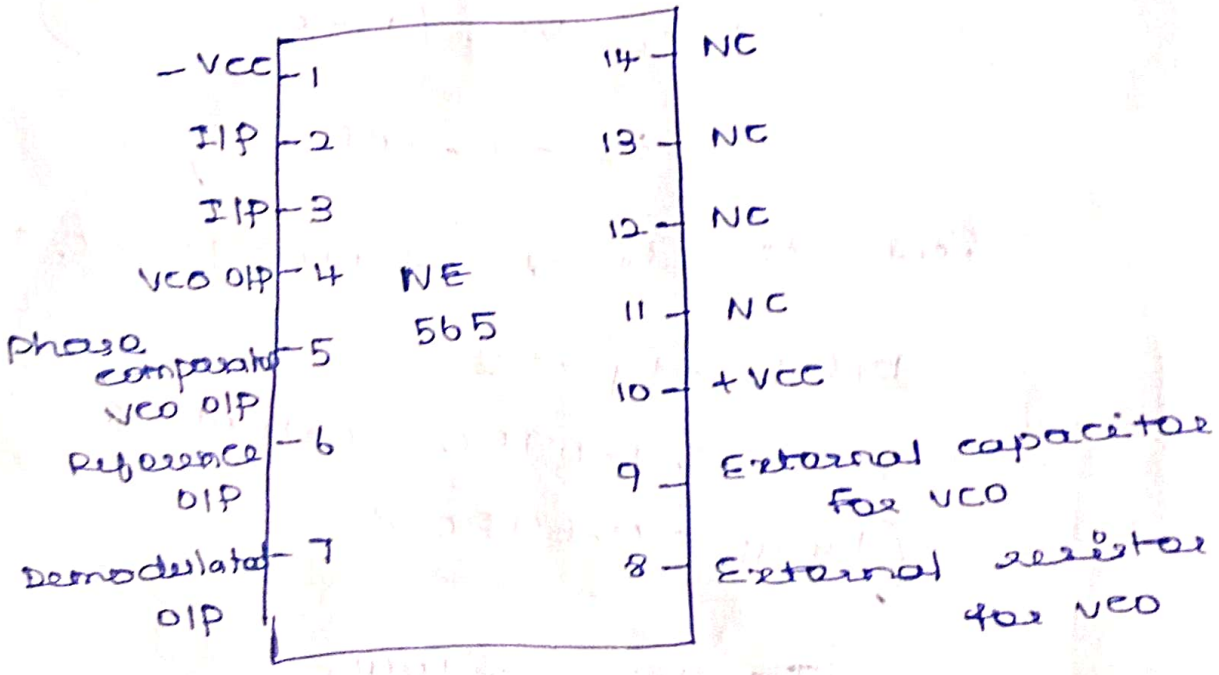
$$\text{Duty cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

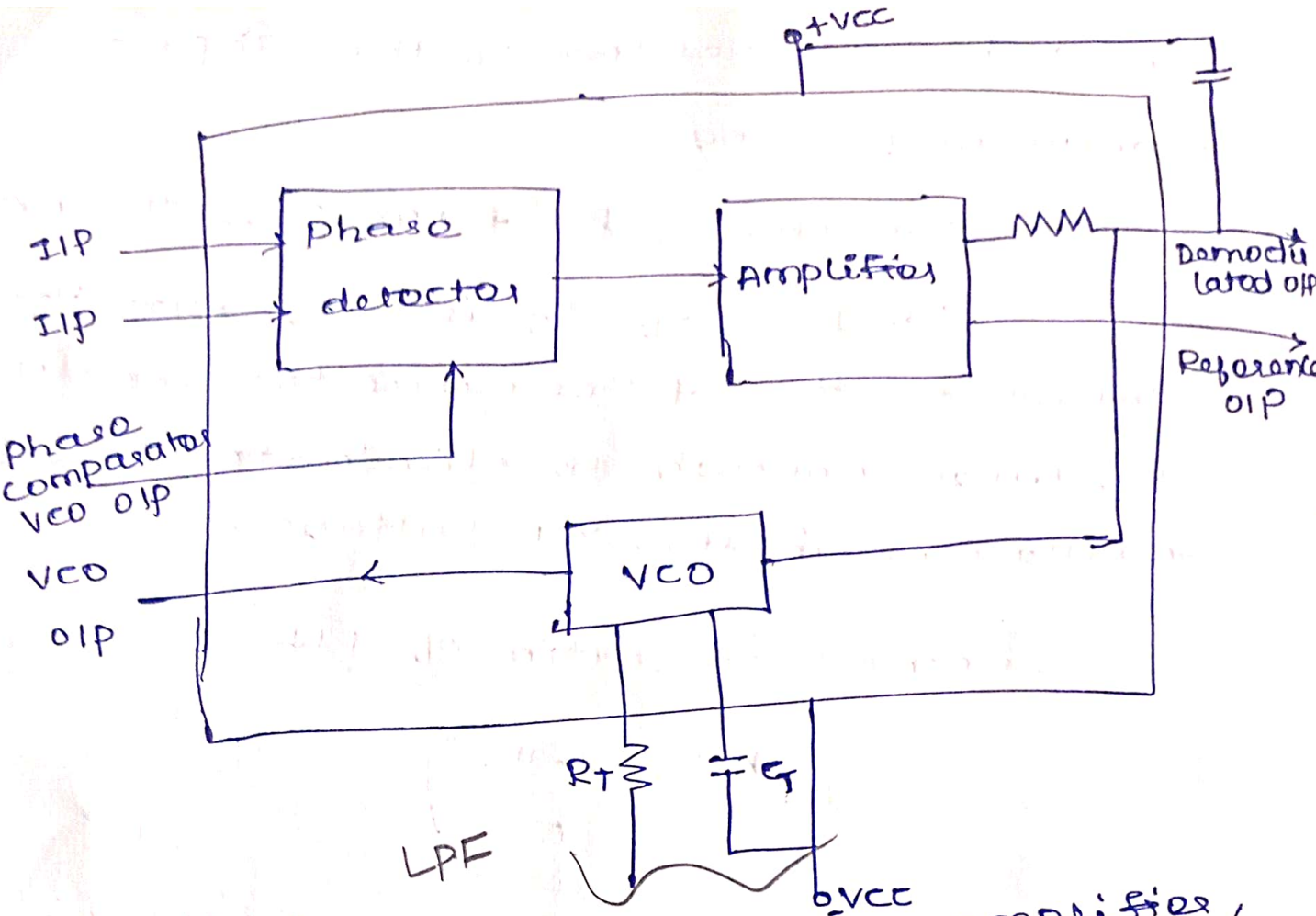
$$= \frac{0.69 R_B C}{0.69(R_A + 2R_B)C}$$

$$= \frac{R_B}{R_A + 2R_B}$$

$$\%D = \frac{R_B}{R_A + 2R_B} \times 100$$

Monolithic PLL IC 565





→ consists of phase detector, amplifier, low pass filter and VCO.

→ phase locked feedback loop is not internally connected.

→ to connect the output of VCO to the I/P of phase comparator.

→ Free running frequency of PLL is determined by the external connected components R_T & C_T.

$$f_0 = \frac{1.2}{4 R_T C_T} \text{ Hz}$$

→ Value of R_T & C_T are adjusted such that the free running frequency

will be at center of the input frequency range.

→ value of R_1 from 2kΩ to 20kΩ

→ value of C_1 is any but the value of the filter capacitor should be large enough to eliminate possible oscillations in the VCO voltage.

→ conversion ratio of PLL

$$K_d = \frac{1.4}{\pi}$$

Voltage controlled oscillator (LM 566)

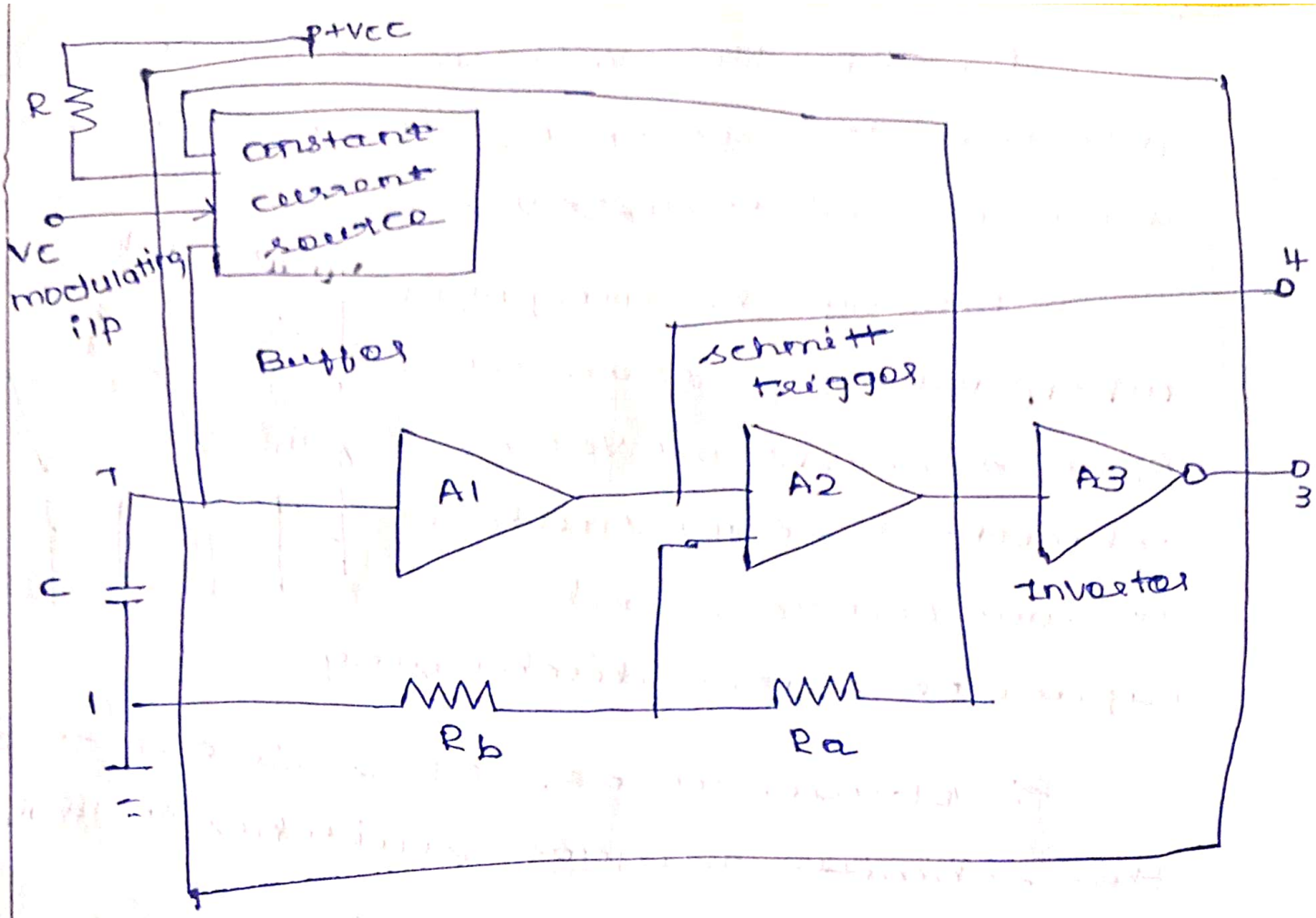
→ Free running oscillator in which frequency of oscillation can be controlled by external timing capacitor, external resistor and externally applied voltage.

→ VCO generates the square and triangular wave forms whose frequency is directly proportional to its control voltage V_C.

→ IC 566, the common type of VCO.

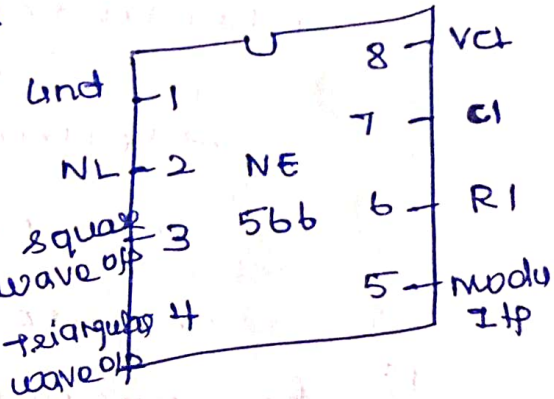
↳ Pin IC

↳ DIP depends on the applied voltage.



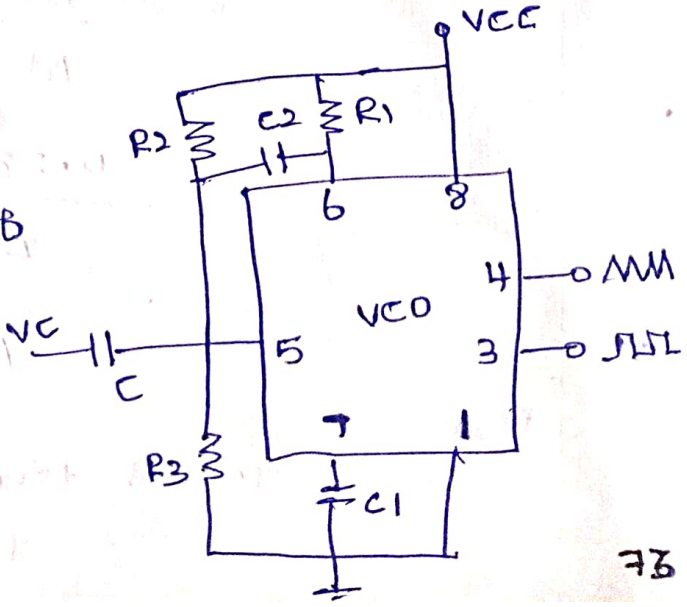
→ constant current source is used to charge and discharge the capacitor C.

→ amount of charge and discharge voltage swing is determined by the schmitt trigger.



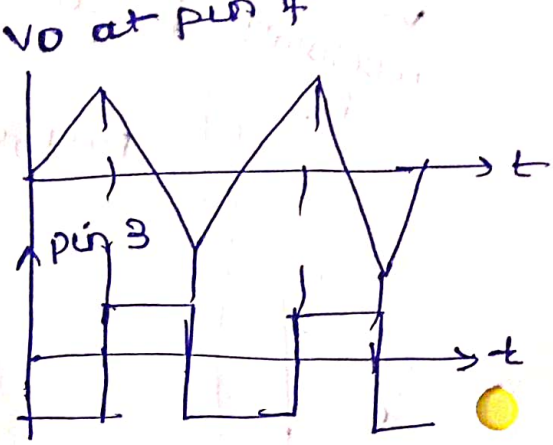
operations

→ o/p voltage swing of schmitt trigger is set to the level Vcc and 0.5Vcc.



→ $R_a = R_b$, the voltage at non inverting terminal of op-amp A2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.

→ During charging of C_1, when voltage across C_1 just exceeds $0.5V_{cc}$, schmitt trigger switches to low ($0.5V_{cc}$) and capacitor starts discharging.



→ voltage across C_1, reduces to $0.25V_{cc}$ the schmitt trigger switches to High (V_{cc})

calculating of Free Running frequency fo

→ voltage change across the C_1 is

$$\Delta V = 0.25 V_{cc} C_1.$$

→ rate of change of voltage across the capacitor is

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_1}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_1}$$

$$\Delta t = \frac{0.25 V_{cc} C_1}{i}$$

total time period $T = 2\Delta t$

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{cc} C_1}$$

$$i = \frac{V_{cc} - V_c}{R_1}$$

$$f_o = \frac{2(V_{cc} - V_c)}{R_1 C_1 V_{cc}}$$

Voltage to frequency conversion factor

$$K_V = \frac{\Delta f_o}{\Delta V_c}$$

ΔV_c – change in modulating signal required to produce a shift frequency Δf.

$$\Delta f = f_1 - f_o$$

$$\Delta f = \frac{2(V_{cc} - V_c + \Delta V_c)}{R_1 C_1 V_{cc}} - \frac{2(V_{cc} - V_c)}{R_1 C_1 V_{cc}}$$

$$\Delta f = \frac{2\Delta V_c}{R_1 C_1 V_{cc}}$$

$$\frac{\Delta f}{\Delta V_c} = K_V = \frac{2}{R_1 C_1 V_{cc}}$$

$$f_o = \frac{1}{4 R_1 C_1}$$

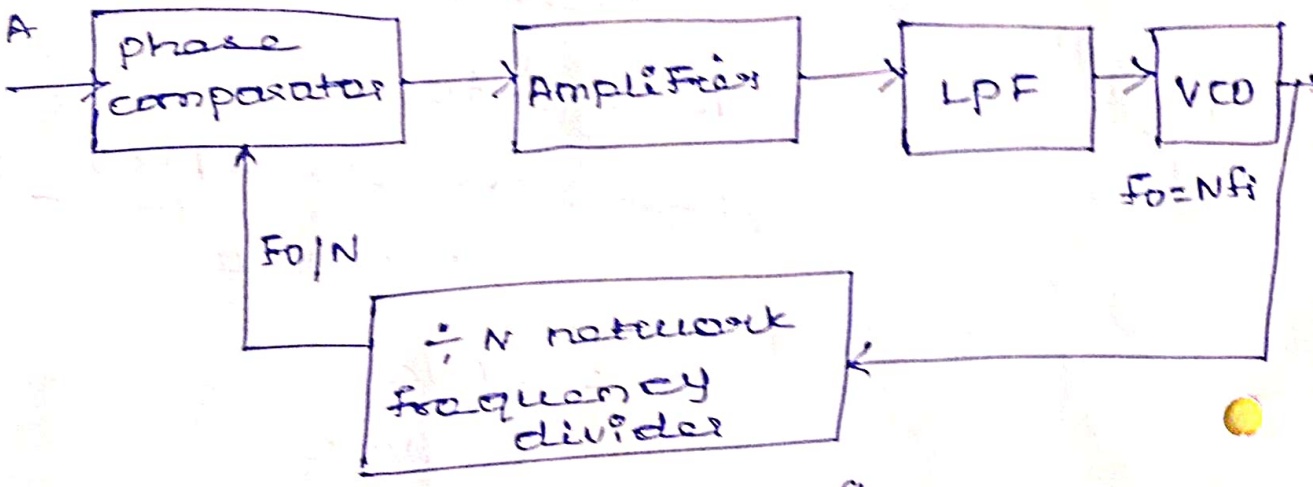
$$R_1 C_1 = \frac{1}{4 f_o}$$

$$K_V = \frac{8 f_o}{V_{cc}}$$

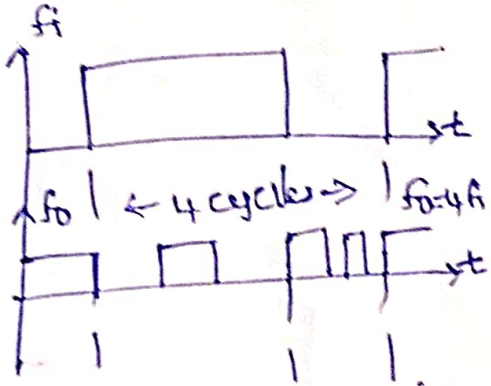
Application of PLL:

- → Frequency multiplication / division
- → AM detector
- → FM detector
- → FSK modulation / demodulation
- → Frequency synthesizing.

Frequency multiplication / division



→ divide by N network is inserted between the VCO & phase detector.



→ PLL is in locked condition the output of the divider is the same as the i/p frequency f_i

→ VCO provides the multiple of the i/p frequency.

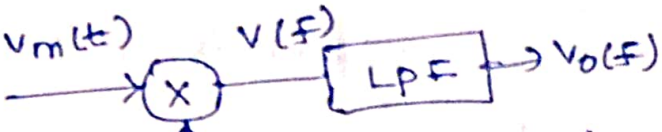
↳ multiplication factor is achieved

by inserting suitable ÷N network

→ N=4 then the cycle of the signal divided into 4 cycles.

AM Detector

→ PLL used in AM detector for demodulating the amplitude modulated signal.



$V_m(t) = V_p(1+m(t))\sin\omega_c t$

$V_c(t) = A\sin(\omega_c t+\theta)$

$V(t) = V_m(t) \cdot V_c(t)$

$= V_p\left[1+m(t)\sin\omega_c t \cdot A\sin(\omega_c t+\theta)\right]$

$= AV_p\left[1+m(t)\sin\omega_c t \cdot \sin(\omega_c t+\theta)\right]$

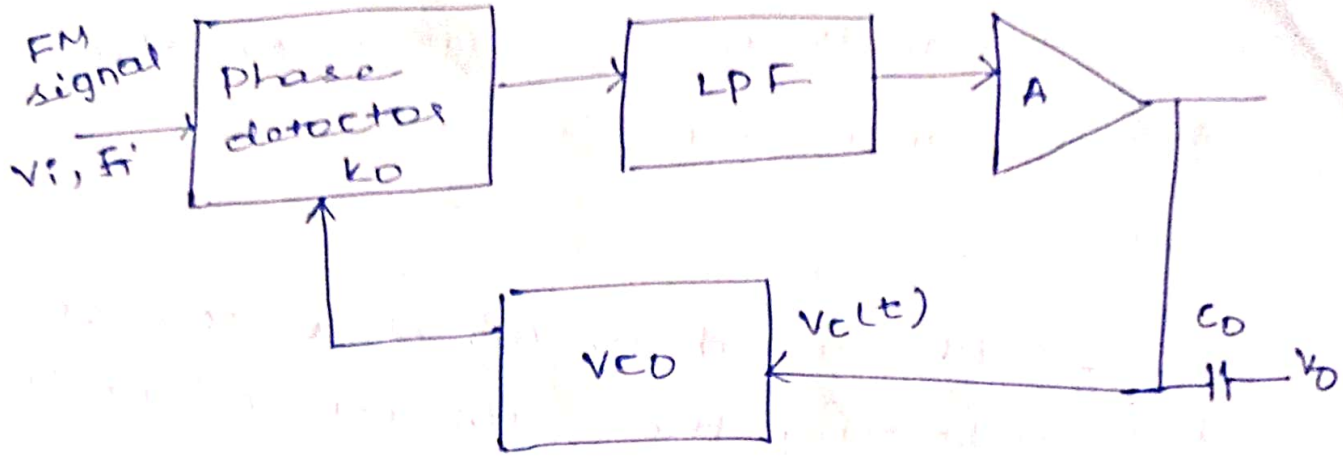
$= AV_p\left[(1+m(t))\left[\frac{\cos\theta - \cos(2\omega_c t+\theta)}{2}\right]\right]$

→ High frequency 2 components can be removed by LPF.

$$V_o(t) = V(1+m(t))\cos\theta$$

FM Detector

→ center frequency f_o should be set as close as possible to the FM carrier frequency f_c to achieve maximum symmetrical lock range.



→ PLL is set locked with the input FM signal.

→ VCO frequency will be equal to the instantaneous frequency of FM signal $f_i(t)$.

$$f_i(t) = f_c + k_o V_c$$

→ VCO control voltage V_c is the demodulated FM output and

$$V_c = \frac{f_i(t) - f_c}{k_o}$$

→ Instantaneous frequency of the FM signal is given by.

$$f_i(t) = f_c + \Delta f_c \sin \omega_m t$$

→ $V_c(t)$ after the capacitor C is

$$V_c(t) = \frac{f_i(t) - f_c}{k_o}$$

$$= \frac{f_c + \Delta f_c \sin \omega_m t - f_c}{k_o}$$

$$V_c(t) = \frac{\Delta F_c}{K_0} \sin \omega_m t$$

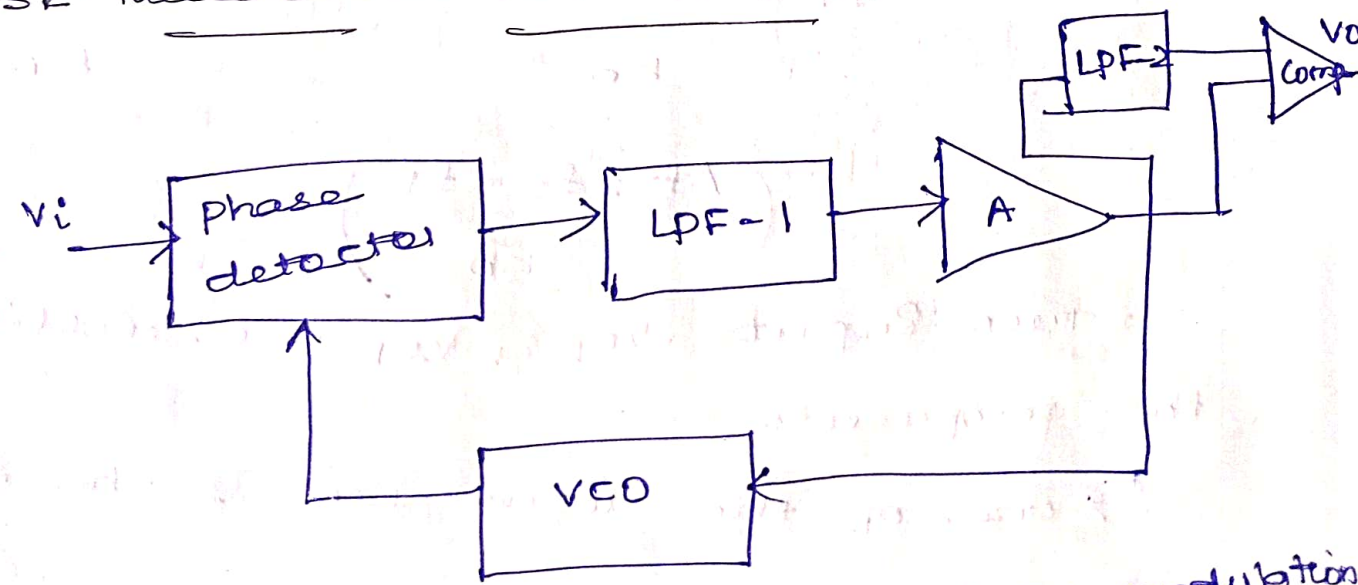
→ control voltage of VCO is linear function of frequency deviation.

↳ FM signal is demodulated, almost without any distortion.

↳ PLL can be employed for detection of wideband or narrowband

↳ FM signals with a higher degree of linearity, which cannot achieved by any other detection methods.

FSK Modulation | Demodulation



→ FSK is a type of frequency modulation in which the binary data code is transmitted by means of carrier frequency that is shifted between two fixed frequency values, namely fi

representing logic 0 and f_c representing logic 1

→ frequency corresponding to logic 1 & logic 0 are called mark and space respectively.

→ PLL is designed to remain in lock with the FSK signal for both the frequencies f_1 & f_2.

→ VCO control voltage f_{cd} to the comparator is given by

$$V_{f1} = \frac{f_1 - f_0}{k_0} \quad , \quad V_{f2} = \frac{f_2 - f_0}{k_0}$$

$$\Delta f = \frac{f_2 - f_1}{k_0}$$

→ Two inputs V_{f1} & V_{f1} are applied to the comparator.

→ one of the input passes through the LPF-2

→ FSK signal V_i is applied to the input, the loop gets locked to input frequency and tracks it in between the two frequencies f_1 & f_2.

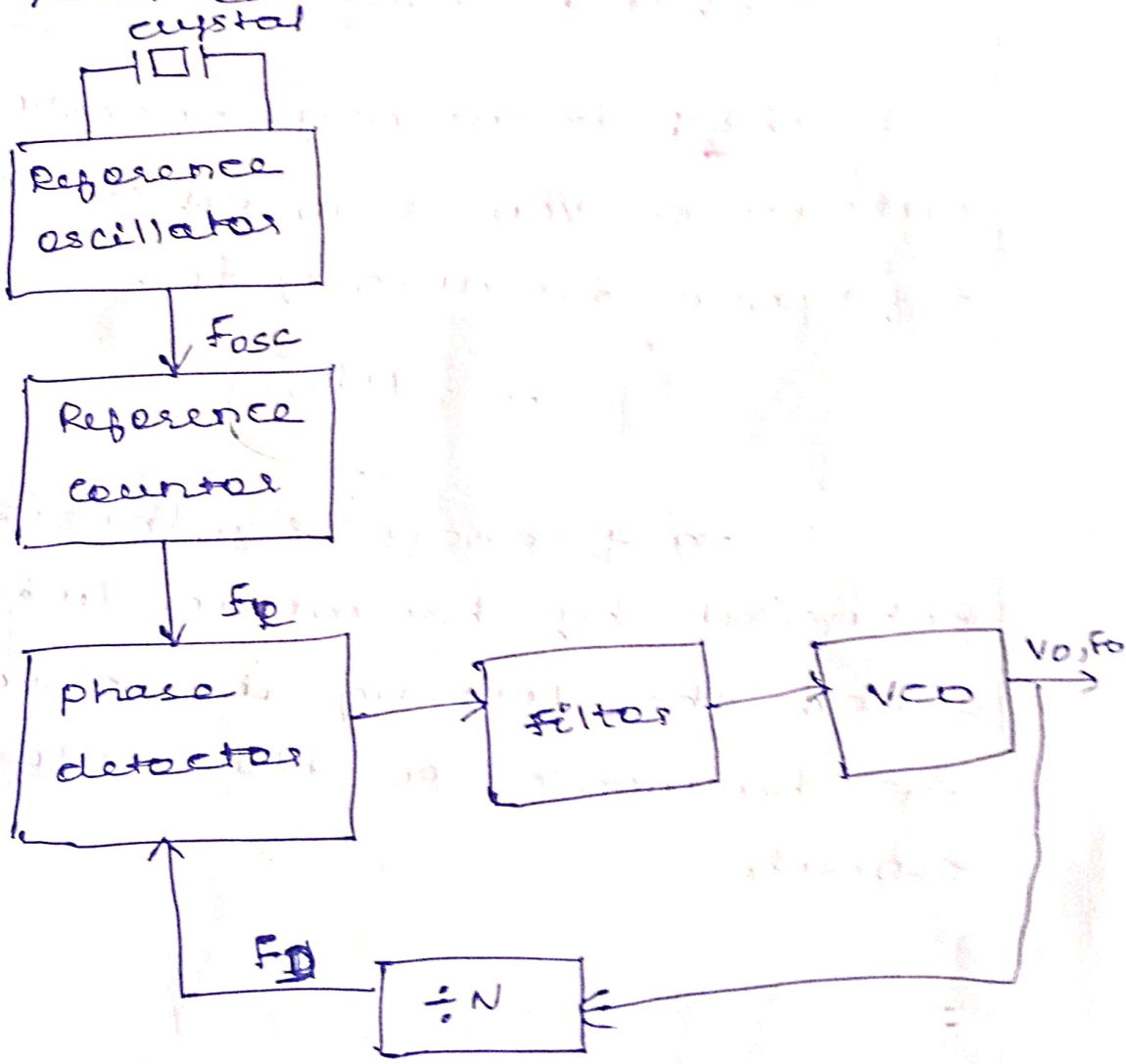
→ Frequency values f_1 & f_2

$$f_1 = \frac{1.45}{(R_A \,||\, R_C + 2R_B)\,C}$$

$$f_2 = \frac{1.45}{(R_A + 2R_B)\,C}$$

Frequency Synthesizing

→ produces a large no of precise frequencies which are derived from crystal controlled oscillators.



→ Crystal oscillator provides reference frequency f_R

↳ second input signal to phase detector is provided by VCO.

↳ divide by N counter is interested in the loop so

$$f_D = \frac{f_0}{N}$$

→ In lock condition $f_R = f_D$

→ O/p frequency observed at the output of VCO is integral multiple of reference frequency f_R.

$$f_0 = N f_D$$

→ Frequency synthesizing can be obtained by harmonic locking in which the locking is achieved with the harmonic of the reference signal.

operation of the basic PLL:

→ PLL is an important building block of linear systems.

→ This technique is used in satellite communication systems, air borne navigation systems, FM communication systems, etc.

Basic principles:

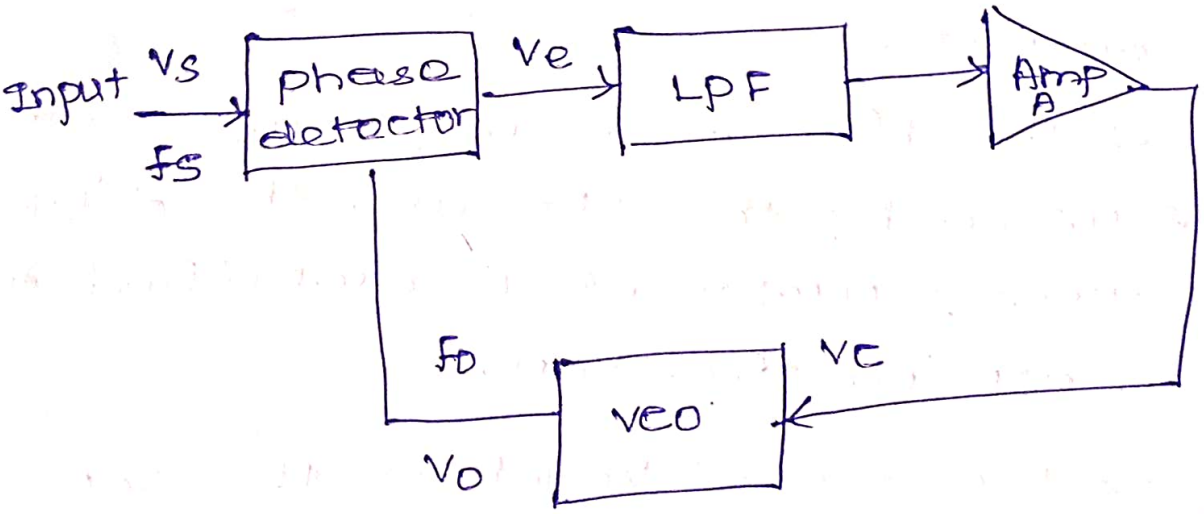
→ This feedback system consists of

↳ phase detector / comparator

↳ A low pass filter

↳ Error amplifier

↳ A voltage controlled oscillator (VCO)



→ The VCO is the free running multivibrator and operates at a set frequency to called free running frequency.

→ This frequency is determined by and external timing capacitor and an external resistor. It can also be shifted to either

side by applying a dc voltage Vc to and appropriate terminal of IC.

→ the frequency deviation is directly proportional to the dc control voltage.

→ If an input signal Vs of frequency fs is applied to PLL, the phase detector compares the phase and frequency of the incoming signal to that of output Vo of the VCO.

→ If the signal differs in frequency or phase and Ve is generated.

→ phase detector is basically a multiplier and produces the sum (fs+fo) and differences (fs-fo) components at its output.

→ the high frequency components (fs+fo) is removed by the LPF and the difference frequency component is amplified and then applied the VCO.

→ the signal Vc shift the VCO frequency in a direction to reduce the frequency difference between fs & fo

→ the VCO continues to change frequency till its output frequency exactly same as the input frequency.

→ once locked, PLL tracks the frequency changes of the output signal.

Three stages,

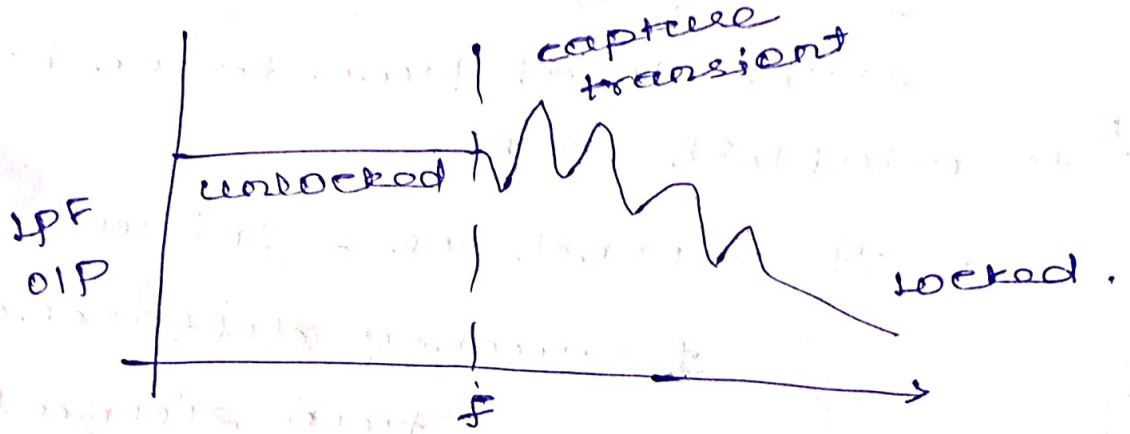
→ Free running

→ capture range

→ locked

Capture Transient

→ As capture starts small sine wave appears. This is due to the differences frequency between VCO and input signal.



→ The dc components drives the VCO towards the lock.

→ The difference in frequency becomes smaller and a larger dc component is passed by the filter, shifting the VCO frequency.

→ The process continues until VCO locks on to the signal and the difference frequency is dc.

Lock in Range:

→ The range of frequencies over which the PLL can maintain lock with the incoming signal.

Capture Range:

→ The range of frequency over which the PLL can acquire lock with an input signal.

Pull in time:

→ The total time taken by the PLL to establish lock.

→ It depends on – Initial phase Ep
frequency difference between
two signal.
– overall loop gain
– loop filter characteristics.

Unit-4

Analog to Digital and Digital to Analog convertors

Introduction

→ Data convertors convert one form of data into another form

→ D/A convertor converts digital data into its equivalent analog data.

→ Analog data required to drive motors and other analog devices.

→ ADC and DAC are also called data converts and they are also available as monolithic integrated circuits.

Specification of DAC

Accuracy:

→ maximum deviation of the output from the ideal value and it is expressed in fraction of LSB.

Linearity

→ Equal increments in the numerical significance of the digital input should result in equal increments in the analog output voltage.

→ actual circuit the I/P O/P relationship is not linear

→ due to voltage across switches.

Resolution:

→ smallest possible change in output voltage.

→ n bit DAC resolution = 2n

$$\% \text{ resolution} = \frac{\text{step size}}{\text{full size}} \times 100$$

→ It also calculated as

$$\% \text{ resolution} = \frac{1}{\text{total no of steps}} \times 100$$

Setting time:

→ Time required for the output of D/A convertor to settle down to within ± (½) LSB of final value after a change in the digital Input.

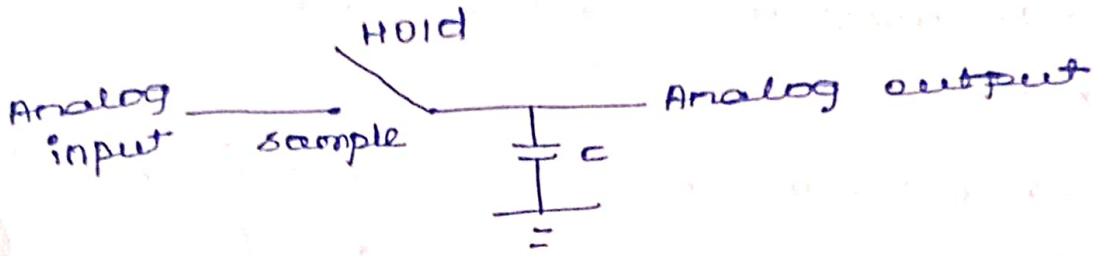
D/A Speed:

→ amount of time required to settle to particular accuracy.

Monotonicity

→ output voltage increases regularly as its binary digital input signal is increased from one value to the next value.

Sample and Hold Circuits (High speed)



→ For accurate analog to digital conversion, the analog input voltage should be held constant during the conversion cycle.

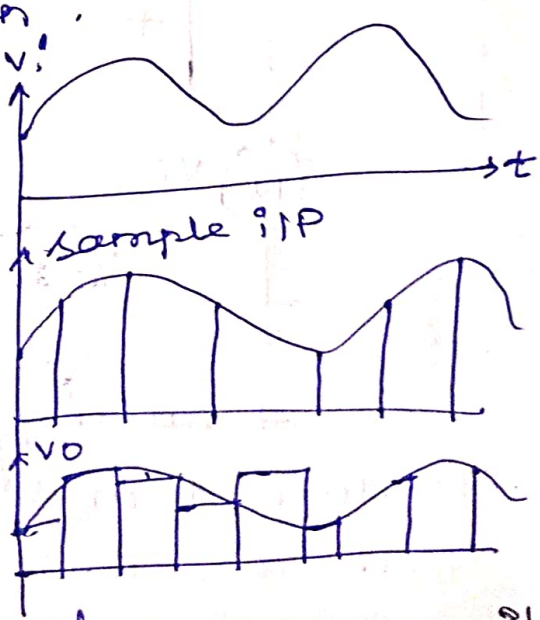
→ analog input voltages changes by more than ± 1/2 LSB n error can occur in the digital output code.

→ To minimize the occurrence of these errors it is necessary to hold the value of analog input voltage constant during the conversion process.

→ Sample and hold circuit, name implies samples an input signal, holds on to its last sampled value until the input is sampled again.

→ samples the analog input voltage in a very short period, generally in the range of 1 to 10 µs

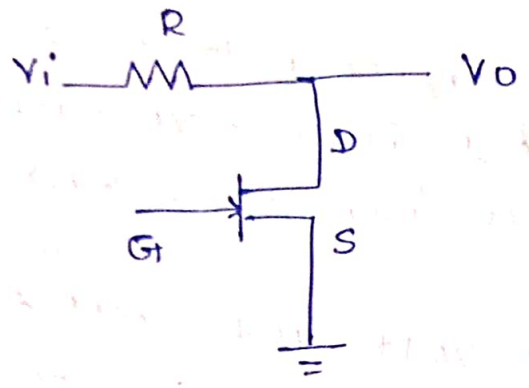
→ holds the sampled voltage level for an extended period, which can range from a few ns to several second.



→ JFET can be used as a switch

→ It may used as shunt or series switch.

Shunt switch

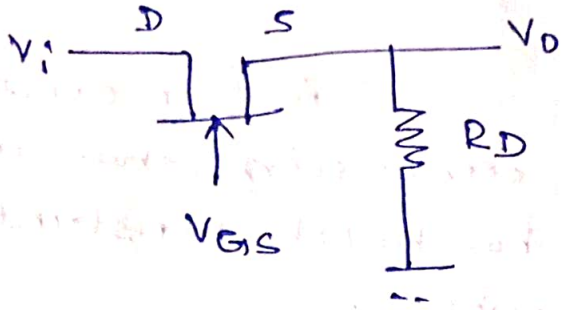


→ $V_{GS} = 0$, JFET acts as closed switch.

→ $V_{GS} = -V_R$, JFET acts as open switch

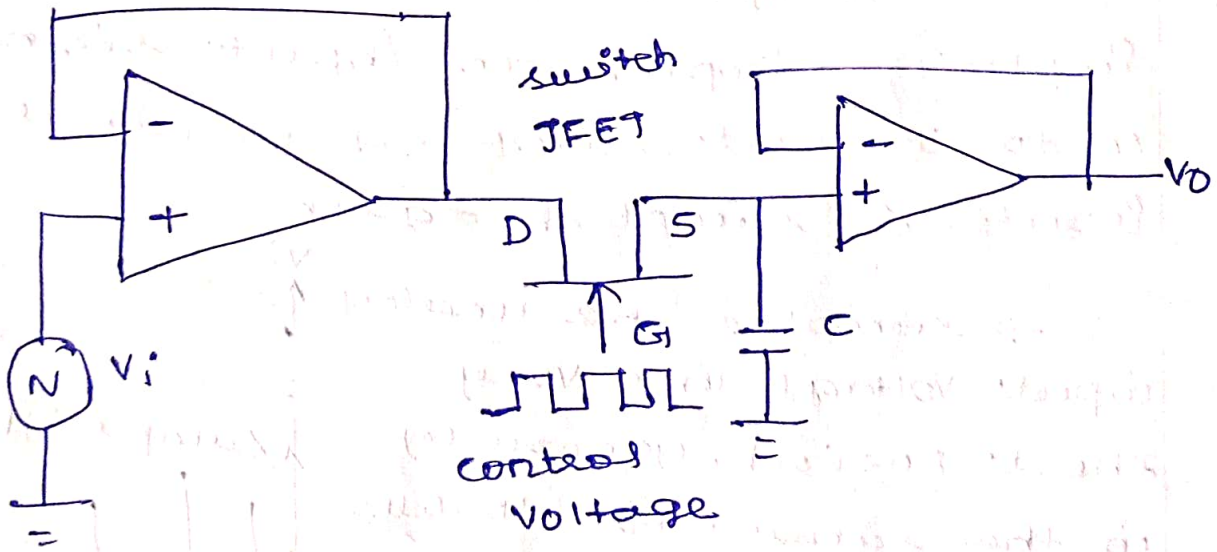
→ $V_O = V_i$

Series switch



→ $V_{GS} = 0$, JFET is closed ∴ $V_O = V_i$

→ $V_{GS} = -V_R$, JFET is open $V_O = 0$



→ During sampling time the JFET switch is turned on the holding capacitor charges upto the level of analog input voltage.

→ At the end of the sampling period the JFET is turned off.

↳ isolates the holding capacitor C_H from the input signal.

→ Voltage across the capacitor C_H & hence the output voltage will remain essentially constant at the value of the input voltages at the end of the sampling time.

→ There will be a small drop off or drop of the capacitor voltage during the hold period due to the various leakage currents to avoid this input and output buffers circuits are used. ie. voltage follower.

Performance

→ Acquisition time (tac)

→ Aperture time (tap)

→ Hold mode setting time (ts)

→ Hold step

→ Voltage DROP

→ Feed through.

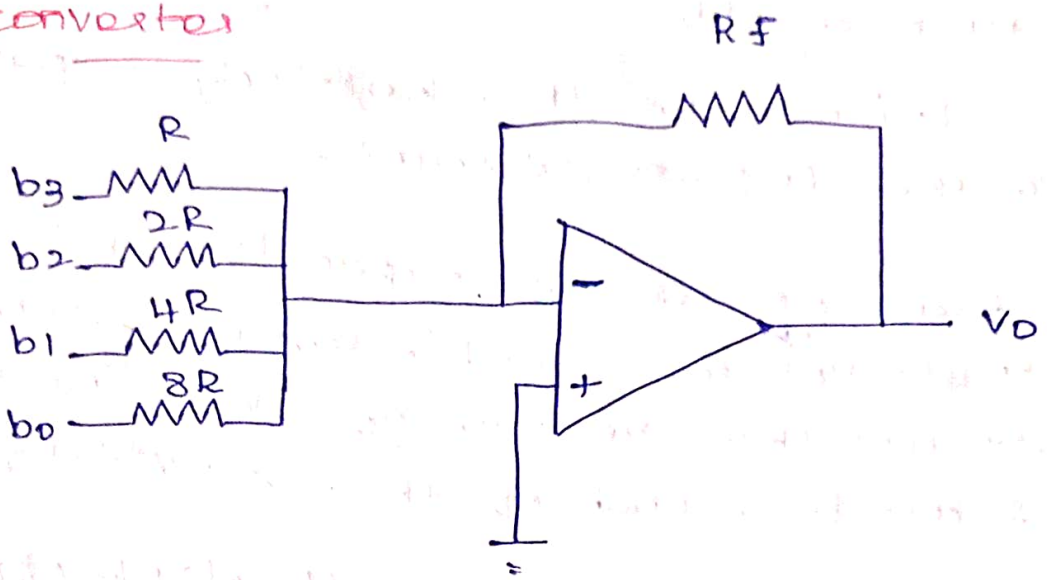
DAC

→ weighted Resistor type.

→ R-2R Ladder type

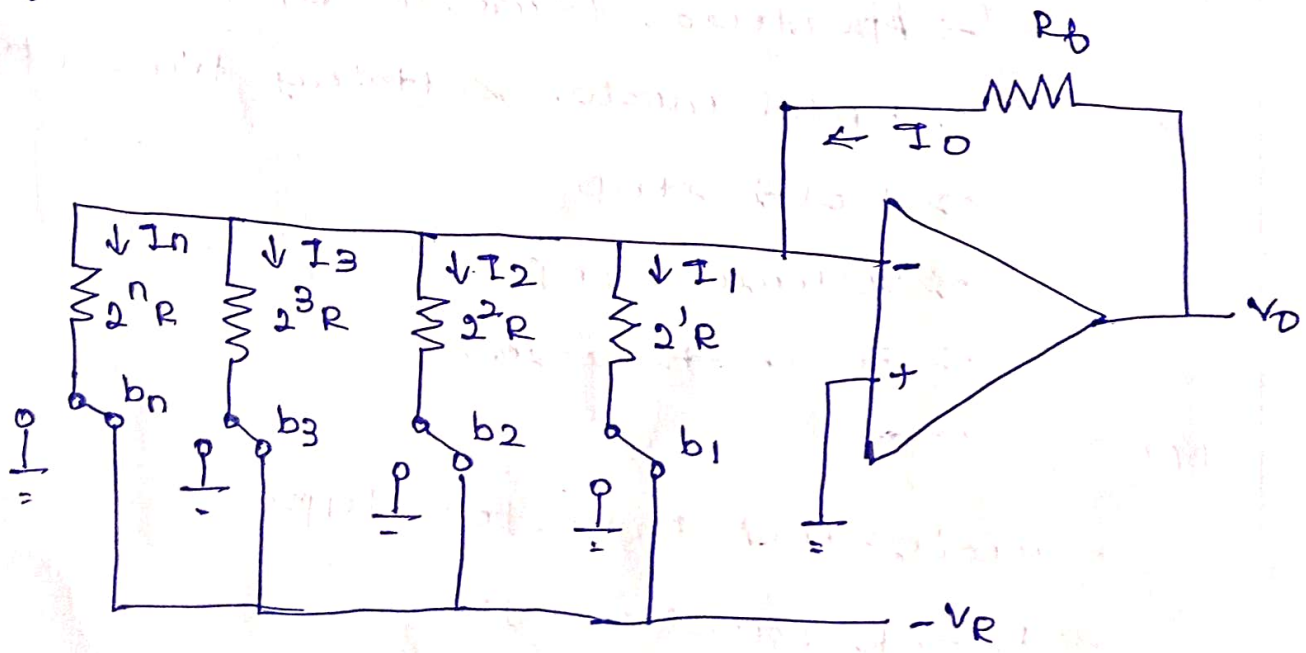
→ Inverted R-2R Ladder type.

Binary weighted resistor type D/A converter



→ Each digital level is converted into n equivalent analog voltage or current.

→ 4 bit DAC which accepts data from 0000 to 1111, there are 15 discrete levels of inputs, and hence it is convenient to divide the output analog signal into 15 levels.



→ n electric switches b1, b2, b3 .. bn controlled by binary input word.

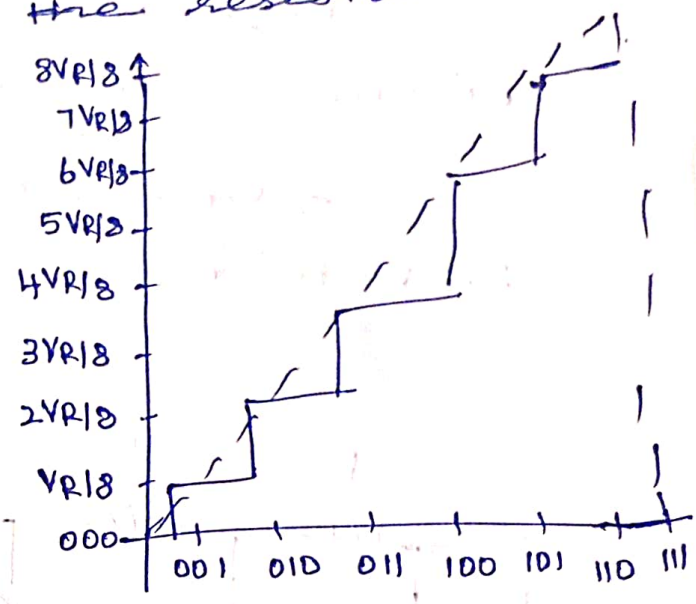
→ switches are SPDT type.

→ binary input to a switch is 1

↳ then the switch connects the resistance to the reference voltage $-V_R$.

→ input bits to the switch is 0

↳ connects the resistor to ground.



$$I_0 = I_1 + I_2 + I_3 + \dots + I_n$$

$$= \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \dots + \frac{V_R}{2^n R} b_n$$

$$I_0 = \frac{V_R}{R}\left[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}\right]$$

output voltage $V_0 = I_0 R_f$

$$V_0 = V_R \frac{R_F}{R}\left[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}\right]$$

$R_f = R$

$$\boxed{V_0 = V_R\left[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}\right]}$$

Disadvantages:

→ wide range of resistor values required

→ better resolution.

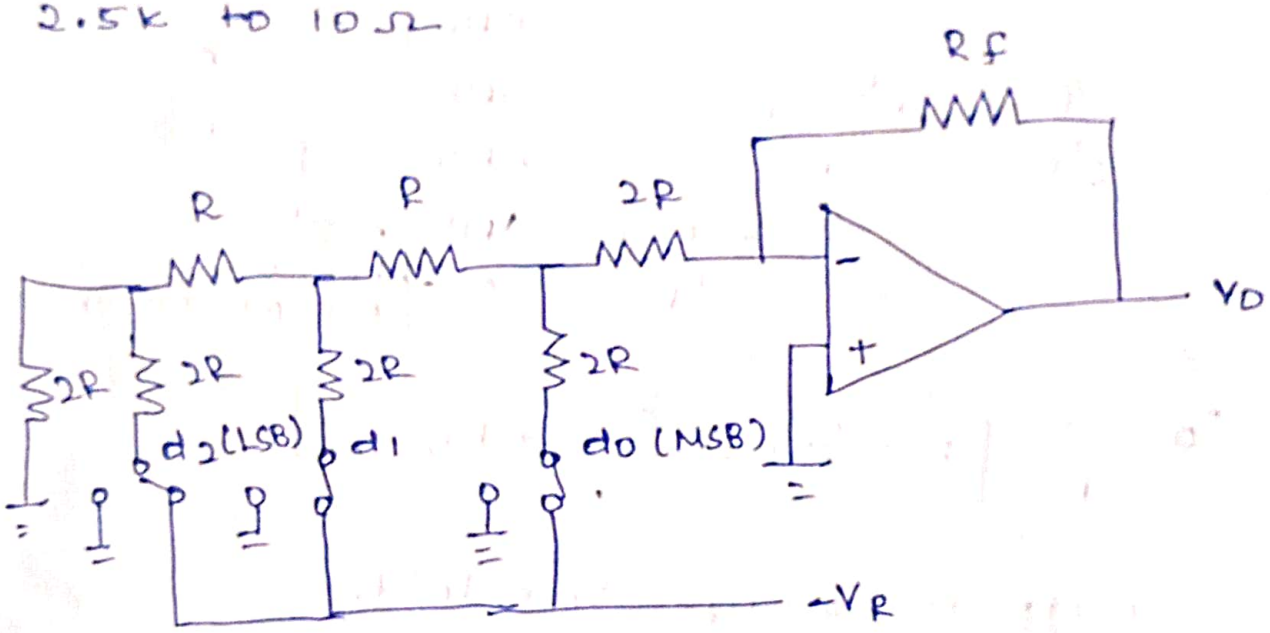
R-2R Ladder DAC

→ wide range of resistors are required in weighted resistor type DAC.

→ R-2R ladder DAC resistor are used only two values R & 2R are used.

↳ It is suitable for integrated circuit realization

→ value of a R ranges from 2.5k to 10Ω

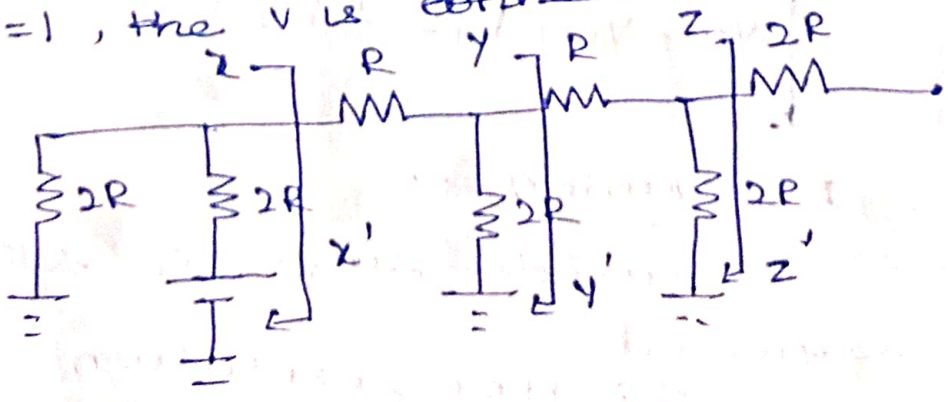


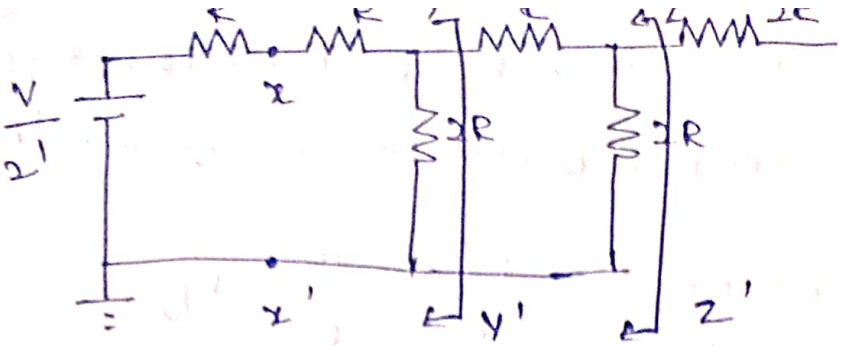
→ 3 bit R-2R ladder DAC.

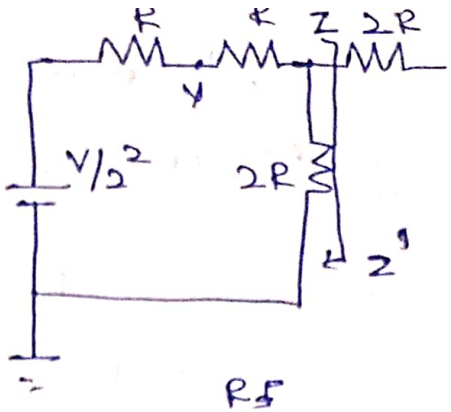
→ To analyse the circuit assume

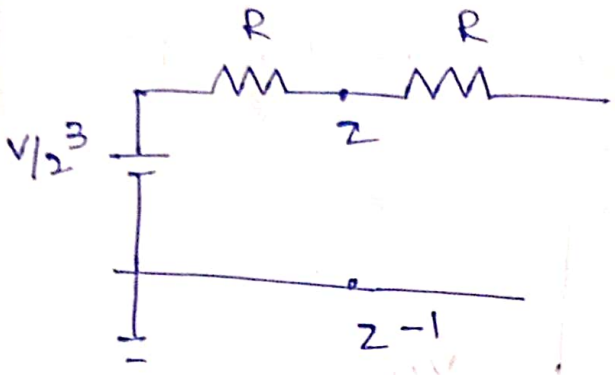
$d_2 d_1 d_0 = 100$

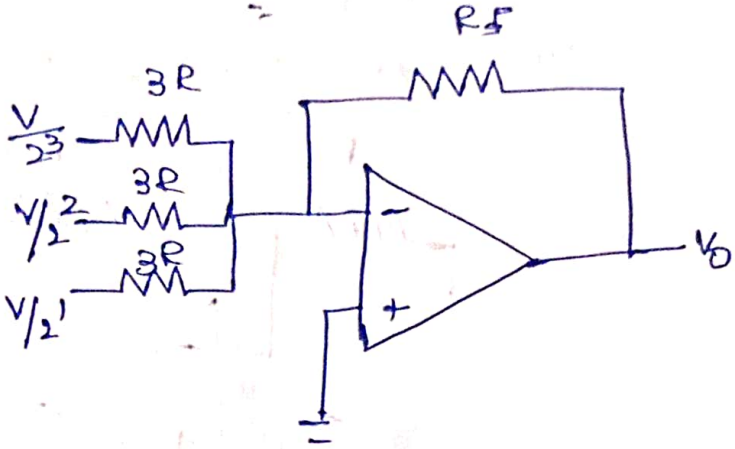
If $d_2 = 1$, the V is connected to d3











$$V_o = \left[\frac{R_f}{3R} \frac{V}{2^3} b_0 + \frac{R_f}{3R} \frac{V}{2^3} b_1 + \frac{R_f}{3R} \frac{V}{2^3} b_2 \right]$$

$$= \frac{R_f}{3R} \left[\frac{V}{2^3} \right] [b_0 + b_1 + b_2]$$

$$V_o = \left(2^0 b_0 + 2^1 b_1 + 2^2 b_2 + \cdots + 2^{N-2} b_{N-2} + 2^{N-1} b_{N-1} \right)$$

$R_f = 3R$, $V = -2^3$

n bit input signal, $R_f = R_1$

$$V_o = -\frac{VR}{2^n} \left(2^0 b_0 + 2^1 b_1 + 2^2 b_2 + \cdots 2^{N-1} b_{N-1} \right)$$

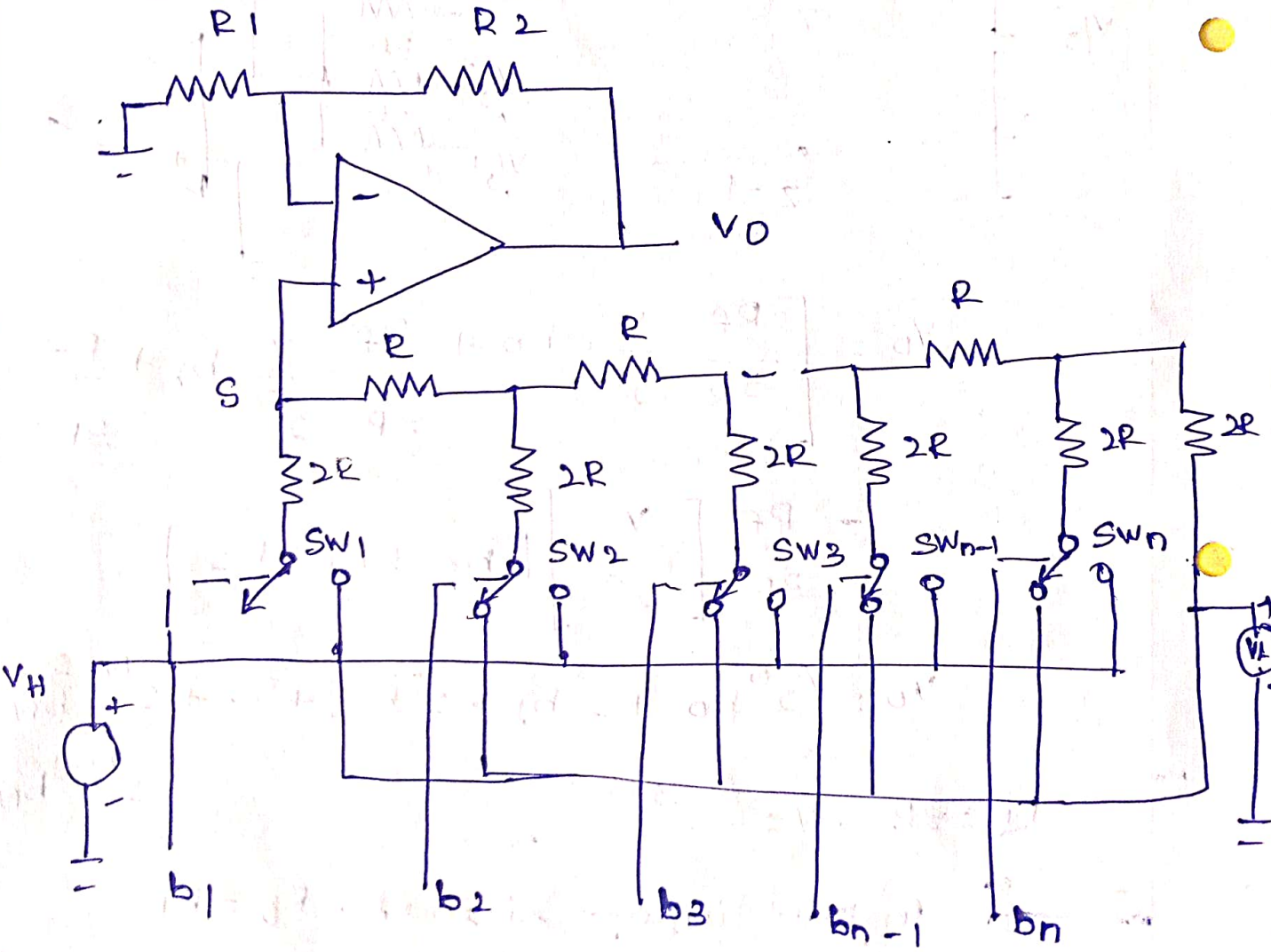
→ Resolution of the R/2R ladder type D/A convertor with current output is given by,

$$\text{Resolution } I = \frac{1}{2^n} \times \frac{VR}{R}$$

→ Resolution of the R/2R ladder type DAC with voltage output is given by

$$\text{Resolution } V = \frac{1}{2^n} \cdot \frac{V_R}{R} \cdot R_f$$

Inverted Voltage mode R-2R Ladder types



→ 2R resistors are switched between the two voltage levels V_L and V_H as determined by the bit values b0, b1 ... bn.

→ output from ladder is obtained at the left most ladder node S and buffered at the output of op-amp.

→ Two voltage V_L & V_H can be any two voltage levels.

→ Input binary word changes from 0 to 1, the voltage of node S changes correspondingly in steps of $2^{-n}(V_H - V_L)$ from the minimum voltage of $V_D = V_L$ to maximum voltage

$$V_D = V_H - 2^{-n}(V_H - V_L)$$

Current Mode R-2R Ladder type

→ weighted resistor and R-2R ladder types of DAC the current through the resistors changes the input data changes.

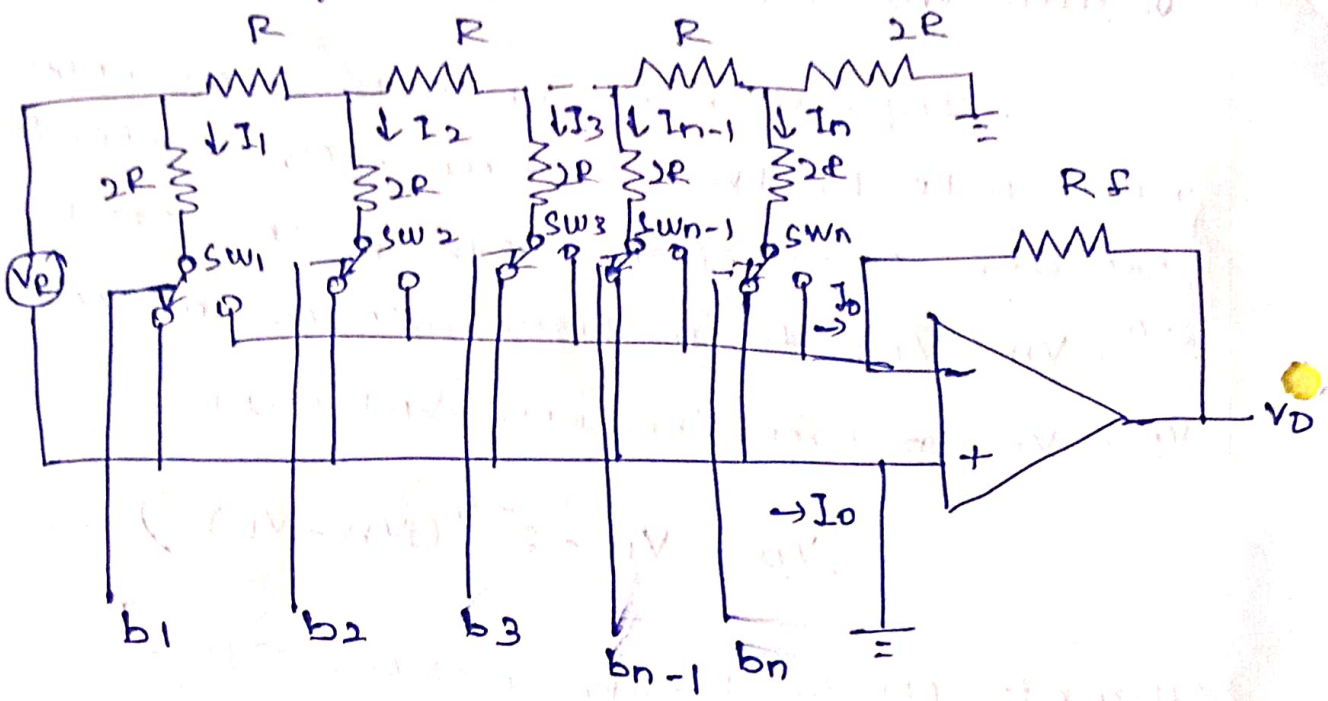
→ power dissipation causes heating and non linearity of DAC arises due to varying power dissipation values corresponding to bit patterns.

↳ because a serious limitation as the word length increases.

→ bit position of each of the subsequent MSB & LSB are interchanged.

→ Each binary input is connected through the switch to either ground or

inverting terminal of op-amp, which is at virtual ground.



→ The current flow through the any resistor is constant.

↳ Independent of the input binary bit value.

⇒ current can be represented as.

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

II^{ly}

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

output voltage $V_o = -I_o R_f$

$= -R_f (I_1 + I_2 + \cdots + I_n)$

$= -\frac{V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n})$

$R_f = R_1$

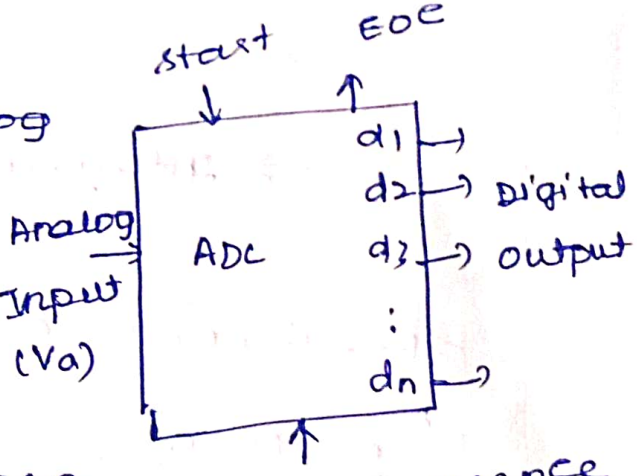
$$V_o = -V_R \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_n}{2^n} \right)$$

→ currents are maintained constant in all branches and the ladder node voltages also remain constants at

$\frac{V_R}{2^0}, \frac{V_R}{2^1} \ldots \frac{V_R}{2^{n-1}}$

A/D convertors.

→ A/D convert an analog voltage to the digital output that best represents the input



↳ Analog convertors are also specified as 8, 10, 12 or 16 bit

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{n}$$

→ It accepts analog input (Va) & produce output binary word $d_1, d_2 \ldots d_n$.

$d_1 = MSB$

$d_n = LSB$

→ Two control lines

↳ start – To tell the ADC when to start the conversion

↳ EOC

↓

Output to announce when the conversion is complete.

Classifications of ADS

→ Direct type – Flash type
– counter type
– servo (or) Tracking counter
– successive approximation type

→ Integrating type – charge balancing
– Dual slope ADC.

specification of ADC

Resolution:

→ smallest change in voltage which may be produced at the output of the converter.

→ ratio of change in the value of input voltage V_i to change the digital output by LSB.

$$\text{Resolution} = \frac{V_{FS}}{2^{n}-1}$$

Linearity

→ Linearity error measures the deviation of actual output from the output taken at that time.

↳ fraction of LSB increment or Percentage of full scale voltage.

Accuracy:

→ maximum deviation between the actual converter output and ideal converter output.

Monotonicity:

→ It is essential in control applications, otherwise oscillation can result.

Setting time:

→ Time required for the output of ADC to settle to within $\pm 1/2$ LSB of the final value for a digital input is zero to full scale.

Stability:

→ The performance of convertor

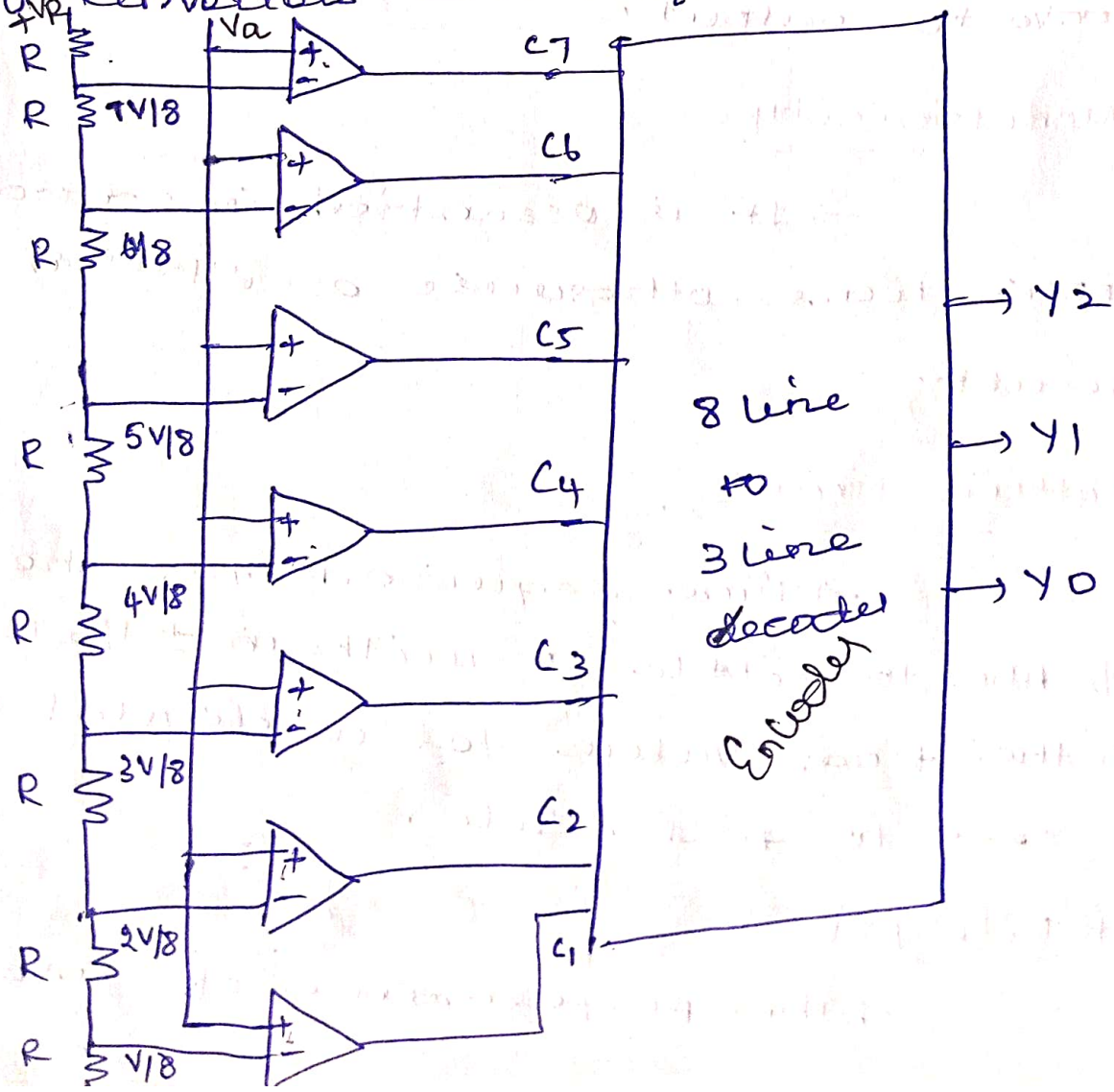
changes with temperature, age and power supply variations.

↳ All the relevant parameters must be specified over the full temperature and power supply ranges.

Flash type ADC

→ This type ADC is based on comparing an unknown analog input voltage with set of reference voltage.

→ To convert analog signal into digital signal of an output bits $(2^n - 1)$ no of comparators are required.



→ circuit requires resistive divider network

→ output of the comparator is in positive saturation o state when the voltage at the non inverting input terminal is more than the voltage at inverting terminal ($V_a > V_d$) and it is negative saturation state otherwise ($V_a < V_d$).

→ comparator and digital outputs for eight different ranges of analog input voltage.

$V_a > V_d$ X = 1

$V_a < V_d$ X = 0

$V_a = V_d$ = previous value

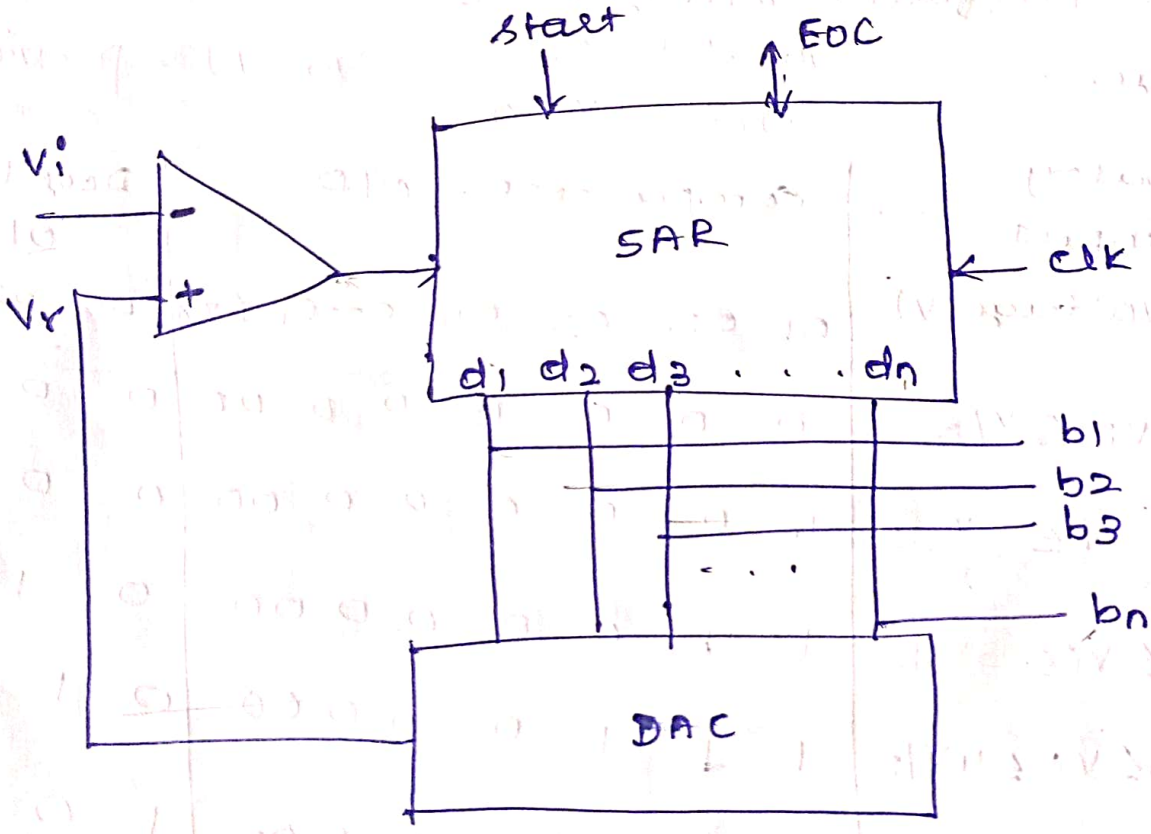
Analog input voltage (V)	comparator O/P							Digital O/P		
	C1	C2	C3	C4	C5	C6	C7	b3	b2	b1
$0 \le V_i \le V/8$	0	0	0	0	0	0	0	0	0	0
$V/8 \le V_i \le \frac{2V}{8}$	1	0	0	0	0	0	0	0	0	1
$2V/8 \le V_i \le 3V/8$	1	1	0	0	0	0	0	0	1	0
$3V/8 \le V_i \le 4V/8$	1	1	1	0	0	0	0	0	1	1
$4V/8 \le V_i \le 5V/8$	1	1	1	1	0	0	0	1	0	0
$5V/8 \le V_i \le 6V/8$	1	1	1	1	1	0	0	1	0	1
$6V/8 \le V_i \le 7V/8$	1	1	1	1	1	1	0	1	1	0
$7V/8 \le V_i \le V$	1	1	1	1	1	1	1	1	1	1

Successive Approximation Type ADC

→ conversion time is maintained constant in successive approximation type

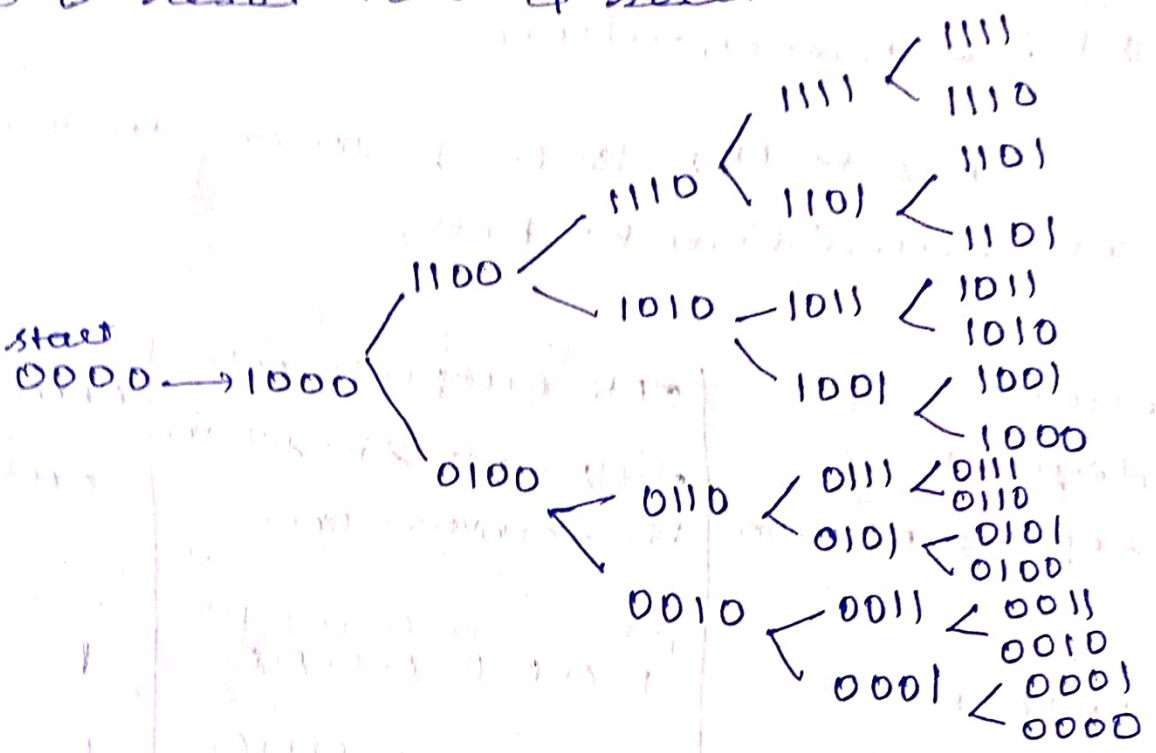
↳ proportional to the no of bits in the digital output.

→ basic principle of this A/D converter is that the unknown analog input voltage is approximation against an n bit digital value by trying one bit at a time, beginning with MSB.



→ MSB is initially set to 1 with remaining three bit 0. The digital equivalent is compared with unknown analog input voltage.

→ analog input voltage is higher than digital equivalent, the MSB is retained as 1 Ep second MSB is set to 1. otherwise the MSB is reset to 0 Ep second MSB is set to 1.



→ This method uses a very efficient code search strategy to complete n bit conversion in just n clock periods.

→ It requires 8 clock period only.

Operation

→ when start command is applied the SAR sets the MSB $d_1 = 1$ with all other bits 0. So the trial code is 10000000. The output of DAC is now compared to V_i

→ If $V_i \geq V_r$ than 10000000 is less than the correct digital representation.

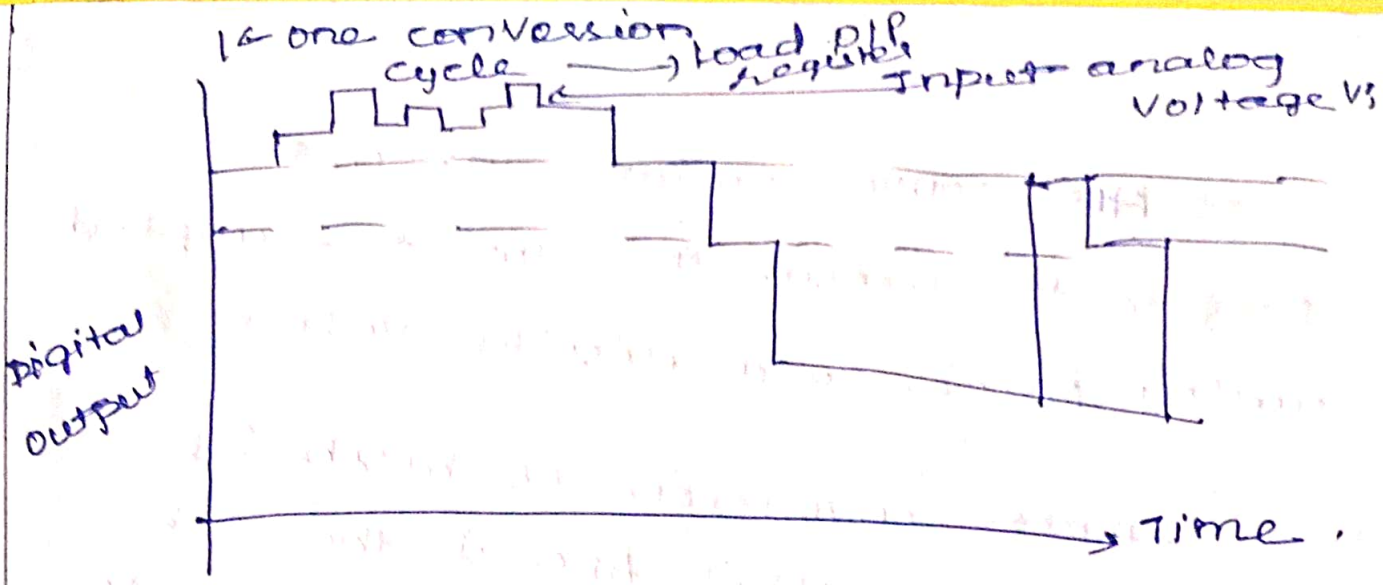
→ MSB is retained as 1 Ep next bit

is made 1 & further tested.

→ ($V_i < V_f$) V_i less than DAC o/p the 10000000 is greater than the correct digital representation

→ Reset MSB to 0 & go on to the next significant bit.

correct digital representation	SAR output at different stages in the conversion.	comparator output
11010100	MSB 0 0 0 0 0 0 LSB	
	1 0 0 0 0 0 0 0	1
	1 1 0 0 0 0 0 0	1
	1 1 1 0 0 0 0 0	0
	1 1 0 1 0 0 0 0	1
	1 1 0 1 1 0 0 0	0
	1 1 0 1 0 1 0 0	1
	1 1 0 1 0 1 1 0	0
	1 1 0 1 0 1 0 1	0
	1 1 0 1 0 1 0 0	—



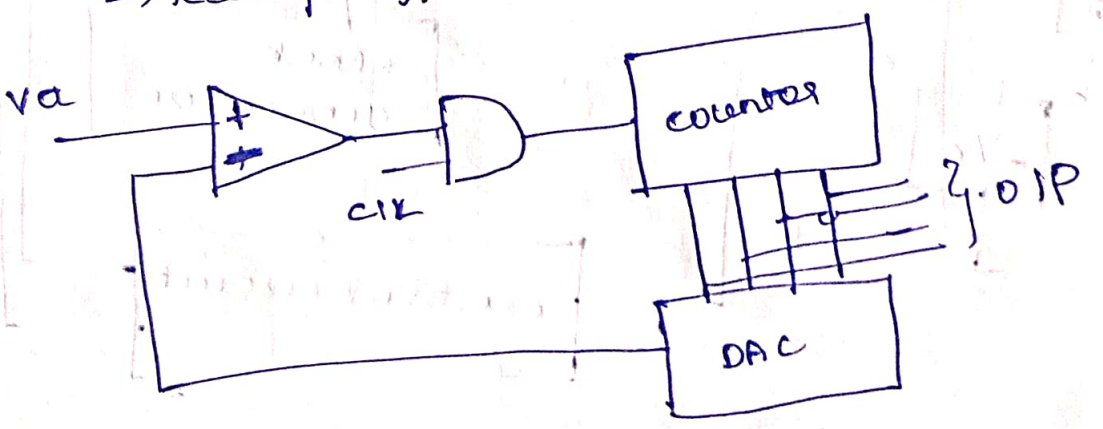
→ D/A output voltage becomes successively closer to the actual analog input voltage.

↳ It requires eight pulses to establish the accurate output regardless of the value of the analog input.

→ one additional clock pulse is used to load the output register and reinitialize the circuit.

Counter type:

→ Ramp type ADC



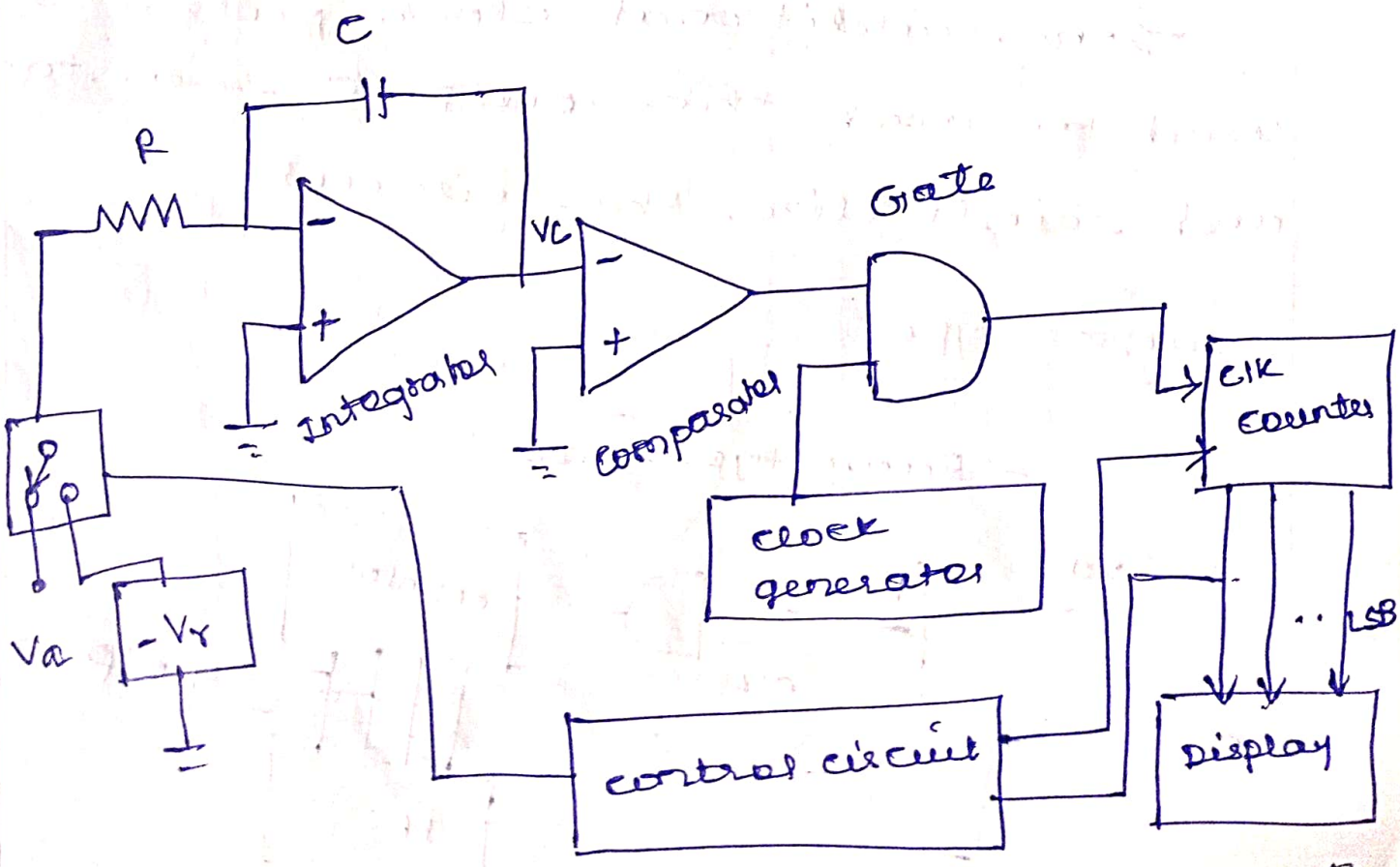
→ ADC conversion time taken the process to change the input sampled analog price to a digital value.

→ most conversions of high i/p voltage for a N bit ADC is the clk pulses necessary to the counter to calculate its maximum count value.

$$(2^N - 1)\,T$$

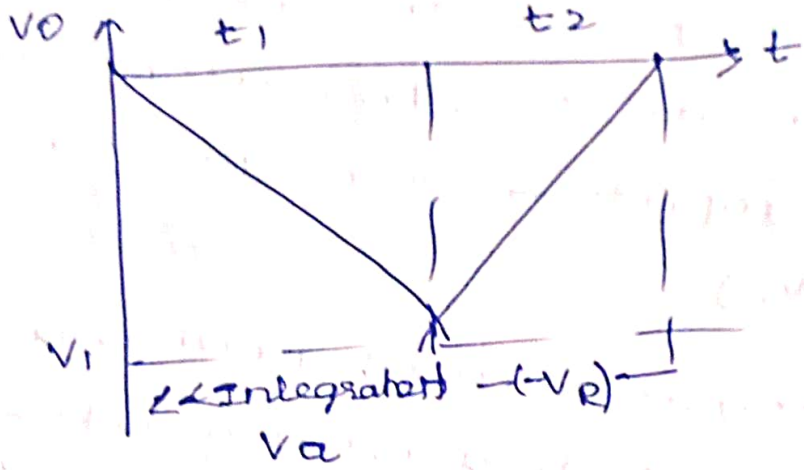
T → time period of the clk

Dual slope A/D convertor



→ consists of integrator, comparator, a binary counter and switch driver.

→ Integrator forms a desired ramp signal. Actually two different ramps are generated, as the input is first switched to the unknown input voltage V_a and then to a known reference voltage V_r.



→ Input is first switched into the unknown input voltage V_a

→ applied input voltage is positive, hence the integrator output voltage V_c will be a negative ramp.

→ comparator output is high (1) and the clock is allowed to pass through the gate to the counter.

→ the ramp is allowed for a fixed period of time t_1 determine by

switch driven for time t_1.

→ Voltage (V_C) developed at the output of the integrator will depend on the unknown input voltage V_a.

$$V_C = -\frac{V_a}{RC} t_1 \quad \text{——— (1)}$$

→ When the counter reaches a fixed count at a time t_1. The control unit generates a pulse to reset the counter to all 0's. And also switch the integrator input to a negative reference voltage ($-V_r$)

→ Integrator will now begin to generate ramp beginning at $-V_C$ & increasing until it reaches 0V.

→ At this time the counter is counting and the conversion cycle ends at 0V.

↳ The comparator output goes to 0 and also the clock gate is now disabled.

$$V_C = \frac{V_r}{R_C} t_2 \quad \text{——— (2)}$$

→ slope of the ramp $\left(\frac{V_r}{RC}\right)$ is constant and time period t_2 is variable.

eqⁿ 1 & 2

$$-\frac{V_a}{RC} t_1 = \frac{V_r}{RC} t_2$$

$$V_a = -V_r \frac{t_2}{t_1}$$

→ V_r - reference voltage.

→ t_1 → pre determined time.

→ V_a - unknown voltage t_2 variable time.

→ unknown voltage directly proportional to the variable time period t_2.

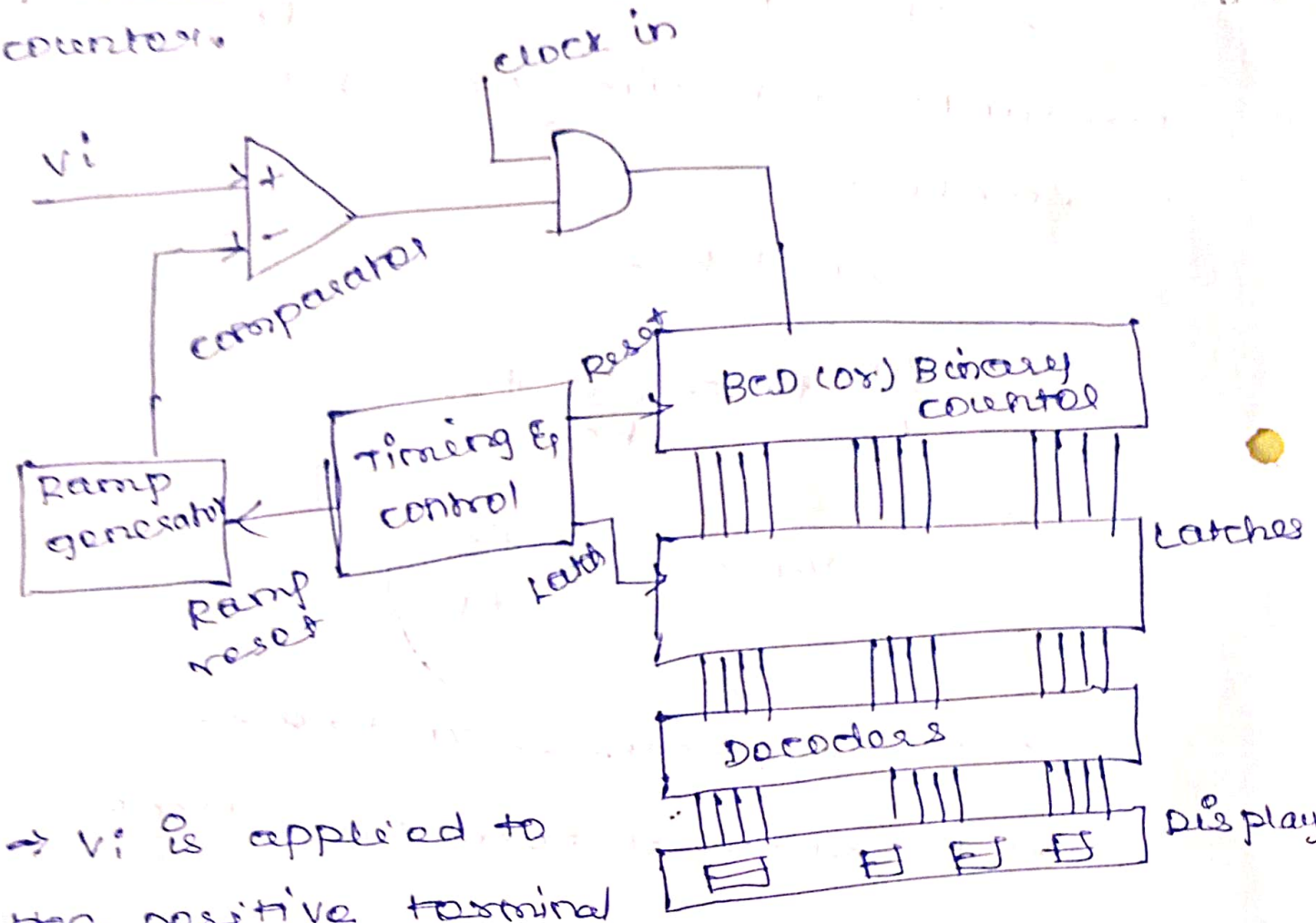
↳ which is exactly equal to the count value of counter at the end of the conversion cycle.

Single slope ADC

→ It consist of ramp generator and BCD or binary counters.

→ At the start reset signal is

provided to the ramp generator and the counters.



→ Vi is applied to the positive terminal of the comparator.

→ If the analog input is more positive than the negative input of the comparator and output goes high.

→ The output of ramp generator is applied to the negative terminal of the comparator.

→ The high output enables the AND gate which allows clock to reach to the counters & this high output starts the ramp.

→ The ramp voltage goes +ve until it exceeds the input voltage. when it exceeds Vi comparator output goes low.

Unit-5

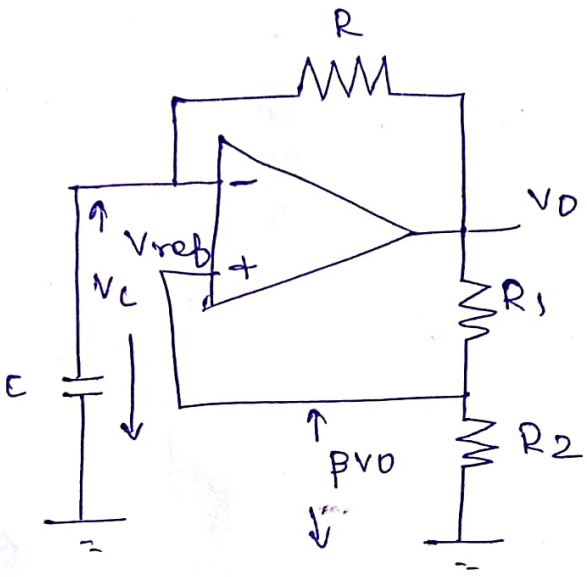
Waveform Generator & Special Function ICs

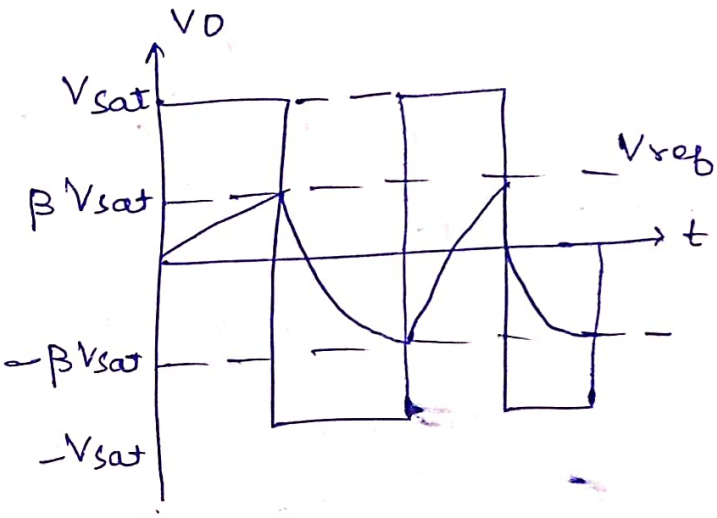
Square Wave Generator

→ Astable multivibrator

→ free running oscillator

→ Two quasi stable state.





→ basically a comparator circuit

→ output goes to either +Vsat (or) -Vsat depending on the differential voltage.

→ potential divider connected across the output terminal, a portion of output voltage (βVsat) is applied to the non inverting input of op-amp

where,

$$\frac{V2}{VO} = \frac{R2}{R1+R2} \qquad \beta = \frac{R2}{R1+R2}$$

$$V_2 = V_0 \left(\frac{R_2}{R_1 + R_2} \right)$$

$$= \beta V_0$$

$$= V_{ref}$$

$$\boxed{V_2 = \beta V_0}$$

→ mismatch between the inverting and non inverting terminal of the op-amp the output goes to either $+V_{sat}$ or $-V_{sat}$.

→ when the supply voltage is switched ON

↳ output goes $+V_{sat}$

→ The capacitor starts charging towards $+V_{sat}$ through R.

↳ The charge on capacitor attains $+\beta V_{sat}$ until it has just exceeded $V_{ref} - \beta V_{sat}$.

→ when the voltage at the inverting terminal becomes just greater than the V_{ref} then the output is driven to $-V_{sat}$.

↳ capacitor begins to discharge through R upto $-\beta V_{sat}$.

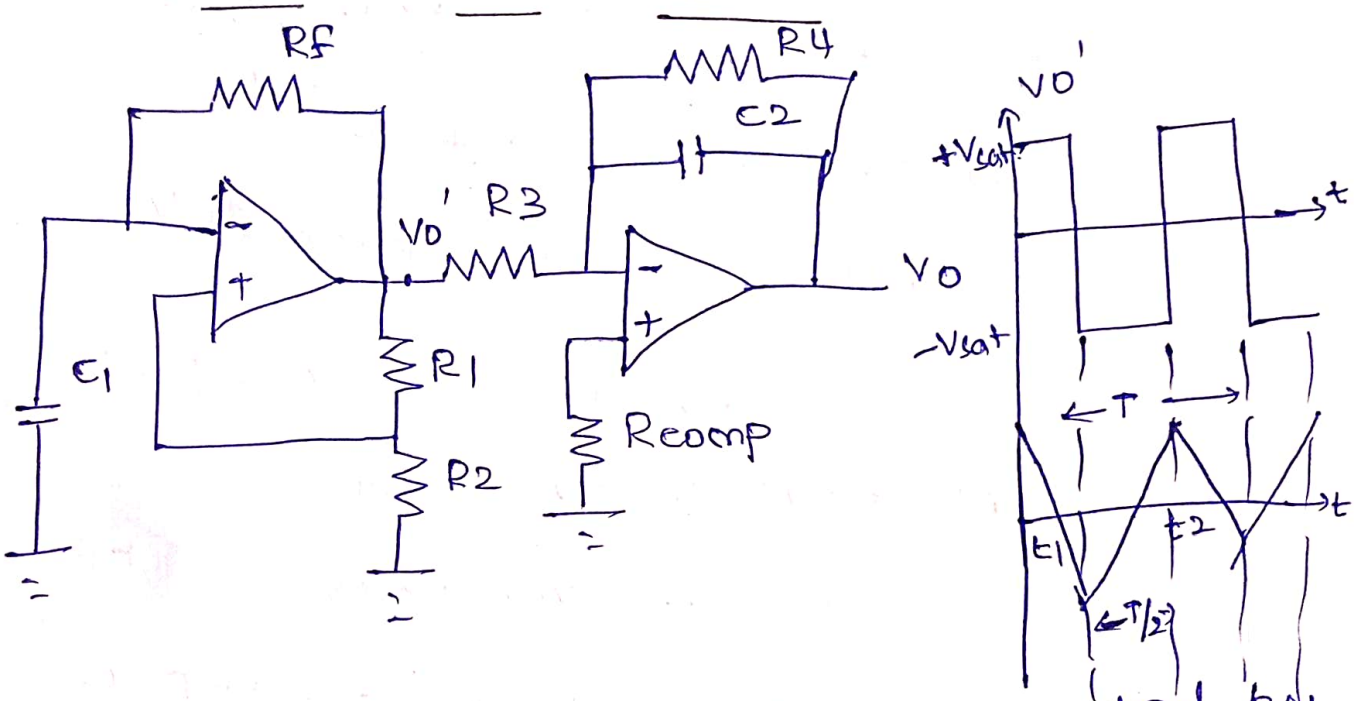
$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Total time period

$$T = 2T_1$$

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Triangular wave Generator



→ Triangular wave is generated by charging and discharging of capacitor with constant current.

→ achieved by connecting integrator circuit at the output of square wave generator.

→ amplitude of square wave generator is constant at ±Vsat. The amplitude of triangular wave will decrease as the frequency increases.

→ output switches back to $+V_{sat}$.

↳ cycle repeats itself.

→ By charging and discharging effect of capacitor, a continuous square wave signal is generated at its output terminal.

→ The voltage across the capacitor is function of time is given by,

$$V_c(t) = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

$$= V_{sat} - V_{sat}(1+\beta) e^{-t/RC}$$

At $t = \pi$, $V_c(t) = \beta V_{sat}$

$$\beta V_{sat} = V_{sat} - V_{sat}(1+\beta) e^{-T1/RC}$$

$$\beta V_{sat} = V_{sat}\left[1 - (1+\beta) e^{-T1/RC}\right]$$

$$\beta = 1 - (1+\beta) e^{-T1/RC}$$

$$\beta - 1 = -(1+\beta) e^{-T1/RC}$$

$$1 - \beta = (1+\beta) e^{-T1/RC}$$

$$\frac{-T1}{RC} = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\frac{T1}{RC} = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

↳ because the reactance of C_2 in the feedback decreases at high frequency.

→ Resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of Practical integrator.

→ $t_1 = t_1$

↳ negative going ramp attains a value of $-V_{ramp}$

↳ switches the output of A1 from positive saturation to negative saturation level $-V_{sat}$.

→ $t = t_2$

↳ switching the output of A1 from $-V_{sat}$ to $+V_{sat}$.

→ The effective voltage, when output of A1 is at $+V_{sat}$ level

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[V_{sat} - (-V_{ramp})\right]$$

$t = t_1$

$$-V_{ramp} = -\frac{R_2}{R_3} V_{sat}$$

$t = t_2$

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

$$= \frac{R_2}{R_3} V_{sat}$$

peak to peak amplitude of triangular wave is.

$$V_{(PP)} = V_{ramp} - (-V_{ramp})$$

$$= \frac{R_2}{R_3} V_{sat} - \left(-\frac{R_2}{R_3} V_{sat}\right)$$

$$= 2\frac{R_2}{R_3} V_{sat}$$

$-V_{ramp}$ to V_{ramp} in half time

period $= T/2$

$$V_o = -\frac{1}{RC}\int V_i \, dt$$

$$V_{(PP)} = -\frac{1}{R_1 C_1}\int_0^{T/2} (-V_{sat})\, dt$$

$$= \frac{V_{sat}}{R_1 C_1}[t)_0^{T/2}$$

$$= \frac{V_{sat}}{R_1 C_1}\left(\frac{T}{2}\right)$$

$$V_{(PP)} = \frac{V_{sat}(T)}{2R_1 C_1}$$

$$T = 2R_1C_1 \frac{V(pp)}{V_{sat}}$$

$$= \frac{2R_1C_1}{V_{sat}} \left(2 \frac{R_2}{R_3} V_{sat} \right)$$

$$T = \frac{4R_1R_2C_1}{R_3}$$

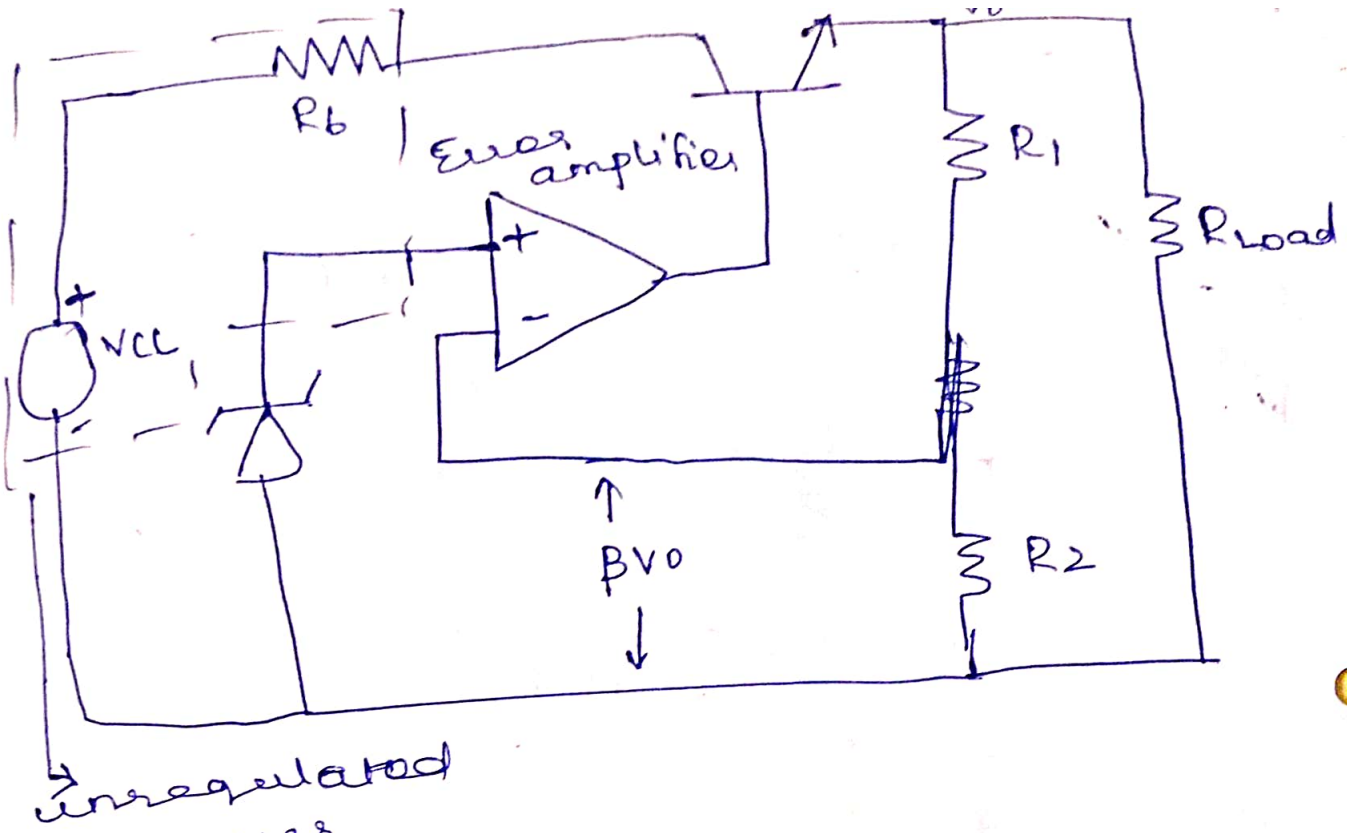
$$f = \frac{1}{T} = \frac{R_3}{4R_1R_2C_1}$$

IC Voltage Regulator

→ Voltage Regulator is an electronic circuit that provides a stable dc voltage independent of load current, temperature and line voltage variations.

→ Regulated power supply using discrete components and the circuit consists of following four parts:

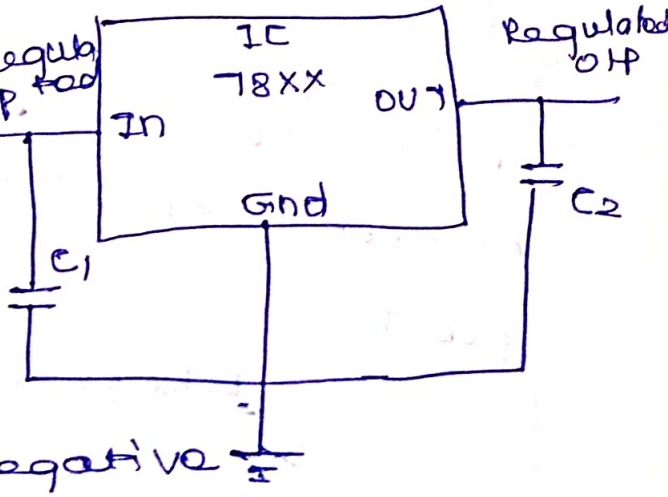
- Reference voltage circuit
- Error amplifier
- Series pass transistor
- Feedback network.



Three terminal fixed and Adjustable voltage Regulators:

→ 78XX series are three terminal, positive fixed voltage regulators

→ There are seven voltage options available such as 5V, 6V, 8V, 12V, 18V & 24V.



→ There are also available 79XX series negative fixed voltage regulator

↳ It is complement to 78XX.

→ two extra voltage also available as -2V & -5.2V in 79XX series.

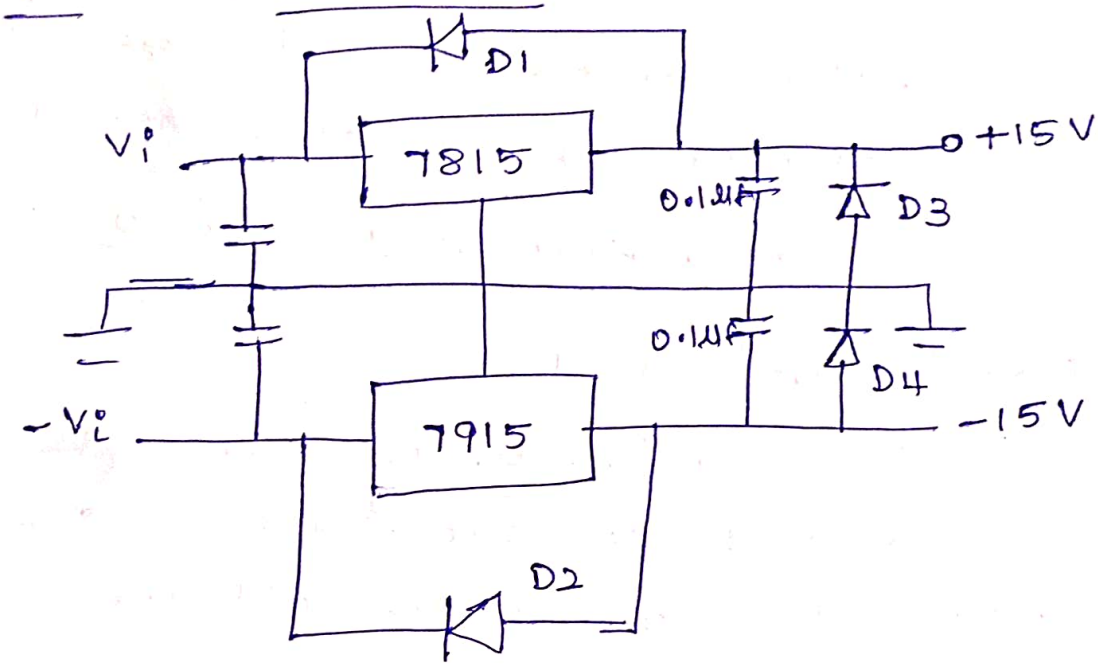
$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_R + R_2 I_Q$$

V_R – regulated voltage difference between the out & GND terminals

LM117, LM217, LM317 – positive regulators

LM137, LM237, LM337 – Negative regulators

Dual voltage Regulator:



→ It is obtained using IC voltage regulators 7815 & 7915

→ 7815 provides +15V output

→ 7915 Provides -15V output

→ The advantage of this method is that it can supply a wide range of voltages at much higher currents with the use of heat sinks and external metal can package pass transistor.

Important parameters

Line / Input regulators:

→ defined as the percentage change in the output voltage for the change in the input voltage

$$\frac{\Delta V_O}{\Delta I_D}$$

Load Regulators

→ defined as the change in output voltage for change in load current.

$$\text{Load regulator} = \frac{\Delta V_O}{\Delta I_D}$$

Ripple Regulation Ratio

→ IC regulator not only keeps the output voltage constant but also reduce the amount of ripple voltage

$$20 \log \frac{V_{ri}}{V_{ro}}$$

Adjustable Regulator

→ one may need variable voltage regulated voltages as a voltage that is not available as standard fixed voltage regulators

$$V_O = V_R + V_{POT}$$

$$= V_R + (I_A + I_{R_1}) R_2$$

$$= V_R + I_A R_2 + V_R / R_1 \, R_2$$

current source, reference amplifier

↳ Error amplifier, a series pass transistor Q1 & R2

$$V_O = V_{ref} \frac{R_2}{R_1 + R_2}$$

→ output voltage is low, then the voltage at INV terminal of error amplifier also low.

↳ This makes the output of error amplifier as more positive.

↳ It makes the Q1 in conduction.

→ It drives more current into the load causing voltage across load to increase.

→ Initial drop on the load voltage has been compensated and any increase in load voltage or changes in the input voltage get regulated.

→ Reference voltage is 7.15 V

$$V_O = 7.15 \left(\frac{R_2}{R_1 + R_2} \right)$$

↳ which will always be less than 7-15 V. so it is used as low voltage regulator (< 7V)

IC 723 General purpose regulator

→ Three terminal regulators have the following limitations.

↳ No short circuit protection

↳ output voltage is fixed.

→ These limitations can be overcome in IC 723, which can be adjusted over a wide range of both positive or negative voltage regulator.

→ This IC is low current device, but can be boosted to provide 5A. It has no inbuilt thermal protection. It has no short circuit current limits.

Features

→ Very low temperature drift

→ High ripple rejection

→ Maximum load current of 150mA

→ Internal power dissipation of 800mW

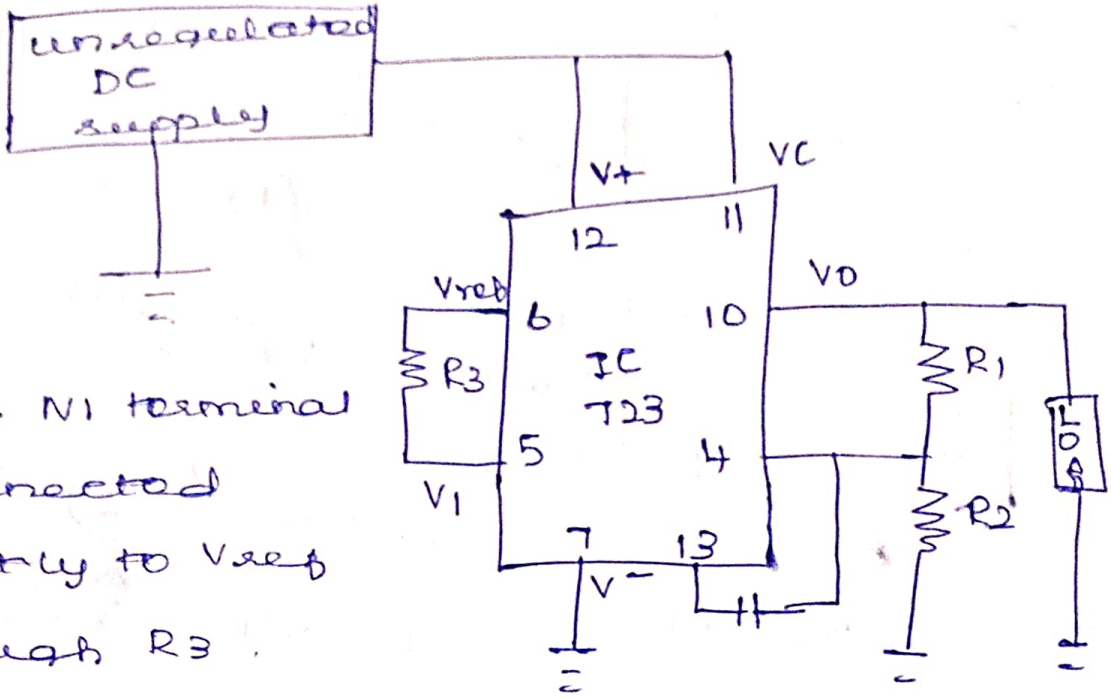
→ Built in short circuit protection and fold back current.

Functional Diagram of 723 regulator

→ Two separate sections

↳ The zener diode, a constant

High Voltage, Voltage regulator using IC 723



→ The NI terminal is connected directly to Vref through R3.

↳ voltage at the NI terminal is Vref

→ Error amplifier operates as a non inverting amplifier with voltage gain of

$$\Delta V = 1 + \frac{R1}{R2}$$

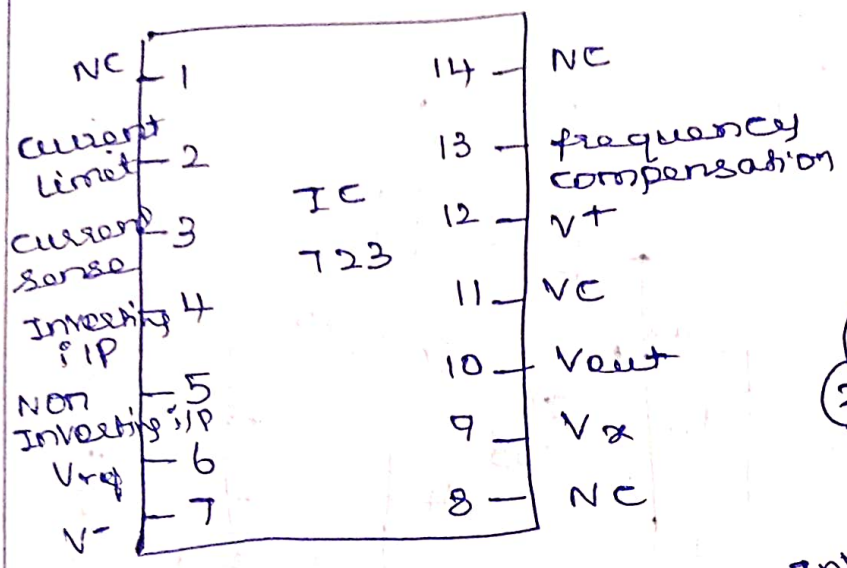
$$V_O = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

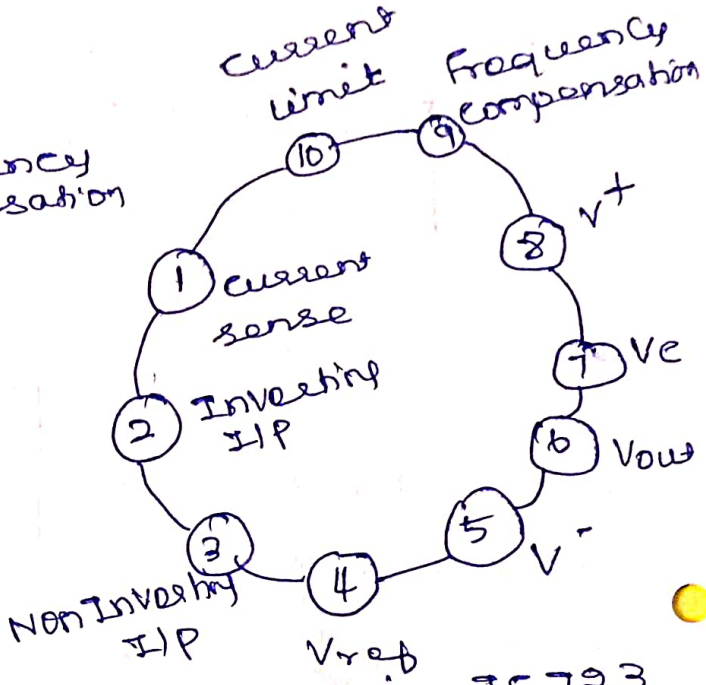
$$= 7.15\left(1 + \frac{R1}{R2}\right)$$

→ Reference amplifier produce a fixed voltage of about 7 volts at the terminal Vref.

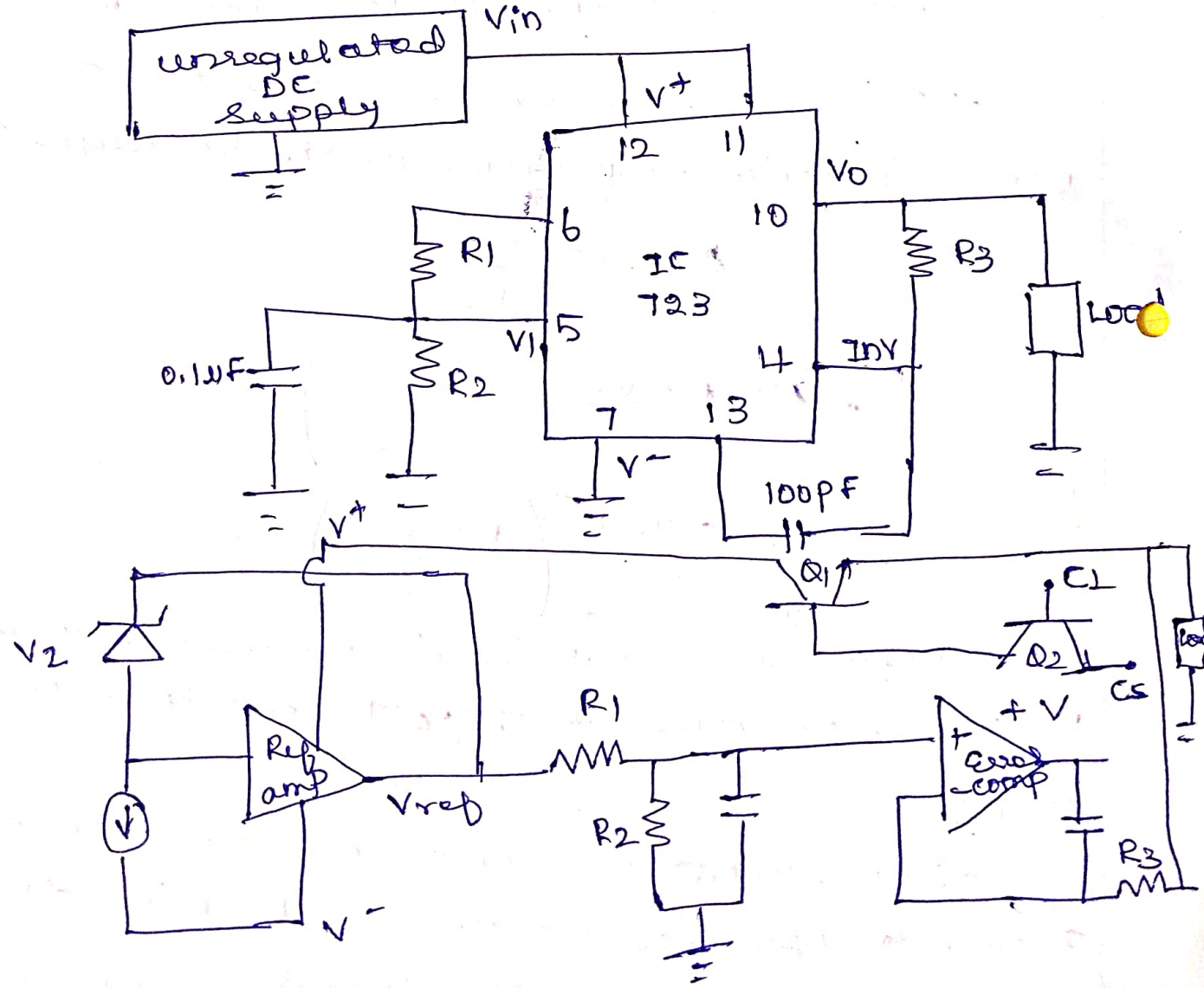
→ constant current source forces the zener to operate at a fixed point so the zener output a fixed voltage.

Pin Diagram





Low Voltage, Voltage regulator using IC 723



→ Voltage at the N1 terminal of the error amplifier due to $R_1 R_2$ divider is

$$V_{N1} = V_{ref} \frac{R_2}{R_1 + R_2}$$

→ Difference between V_{N1} & the output voltage V_o which is directly feedback to the INV terminal is amplified by error amplifier.

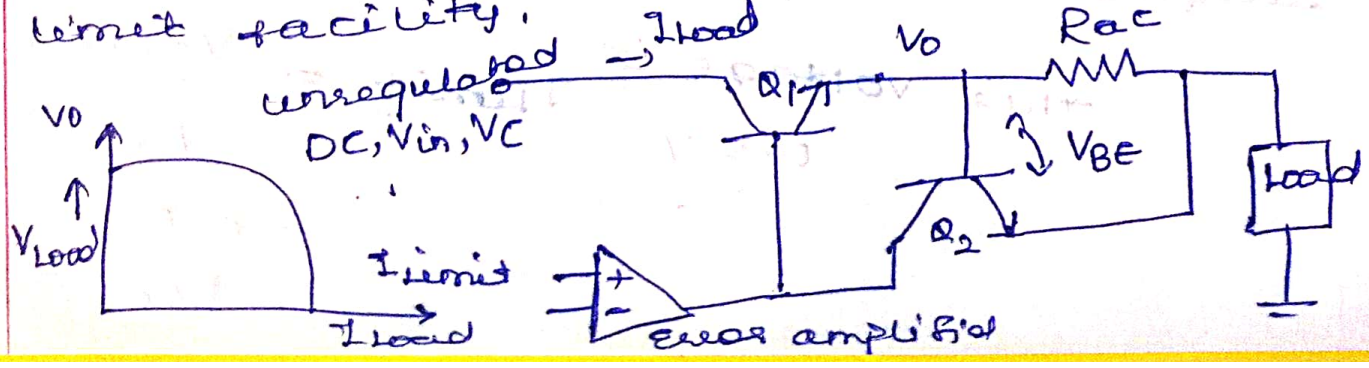
Protection circuit in Regulators

→ current limit protection
→ current foldback
→ current boosting.

current limit protection

→ If the load demands more current eg. under short circuit conditions, the IC tries to provide to it at a constant output voltage getting hotter all the time.

→ IC is provided with a current limit facility.



→ To ability of regulator to prevent the load current from increasing above present value.

→ output voltage remains constant for load current below I_{limit}.

→ current limit I_{limit} is set by connecting an external Resistor R_{SC} between the terminal C_L & C_S.

↳ C_L is connected to the output voltage V_o

↳ C_S terminal to the Load.

→ The load current produces a small voltage drop V_{sense} across R_{SC}.

↳ It is applied directly across the base emitter of Q_2.

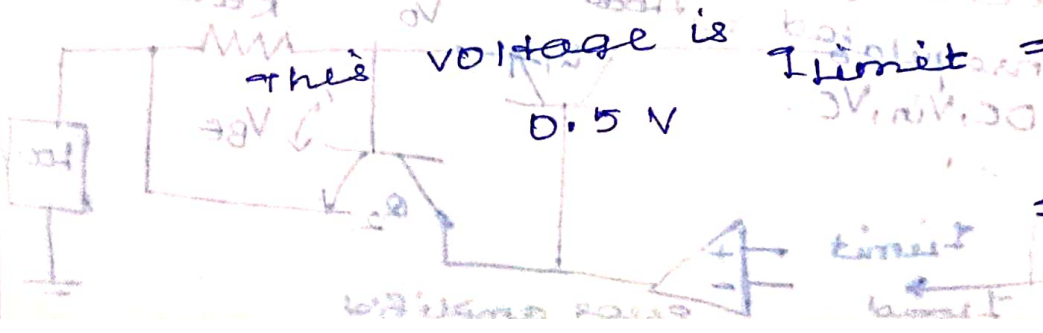
→ If load current decreases, V_{BE} of Q_2 drops.

↳ The load current is held constant to produce voltage across R_{SC} sufficient to turn ON Q_2.

This voltage is 0.5 V

$$I_{limit} = \frac{V_{sense}}{R_{SC}}$$

$$= \frac{0.5\,V}{R_{SC}}$$



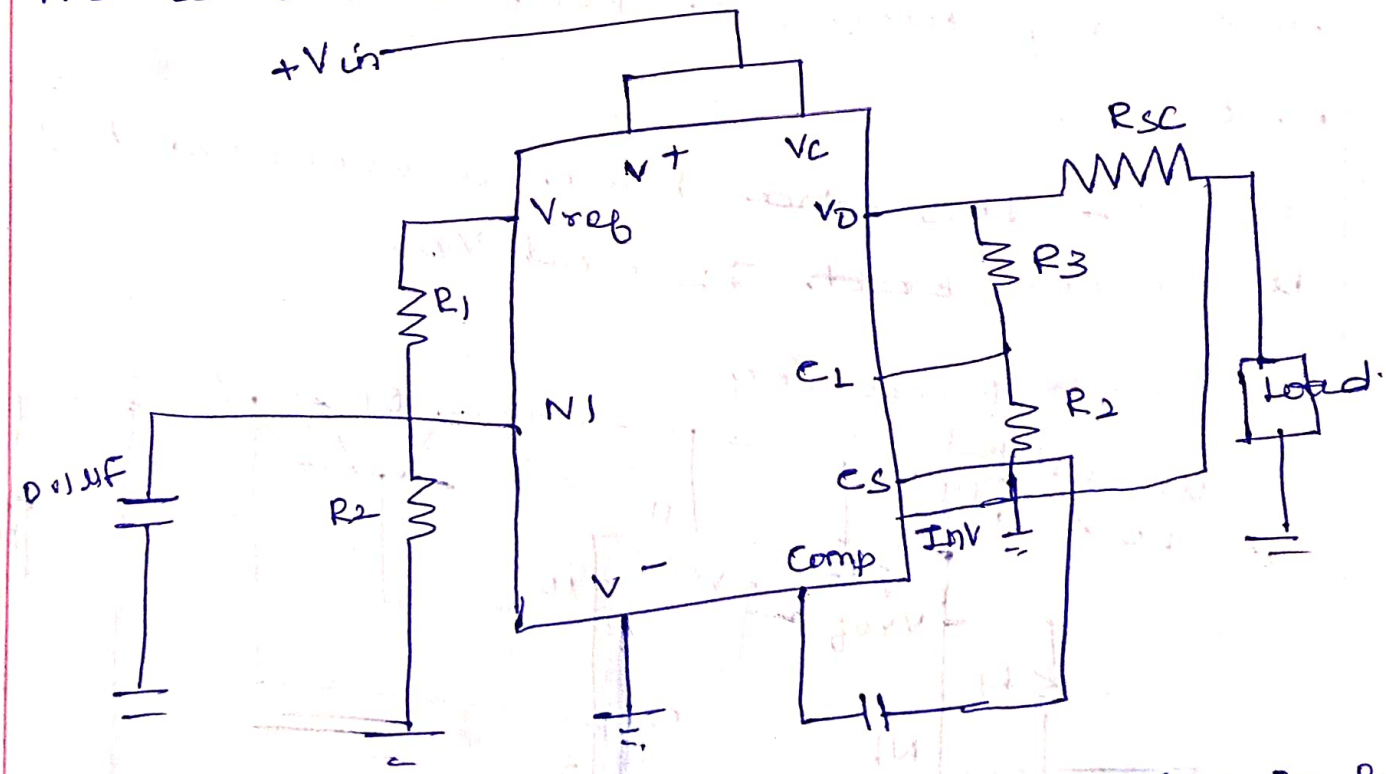
current foldback

→ In current limiting technique, the load current is maintained at present value and when overload condition occurs.

↳ the output voltage drops to zero.

→ Load is short circuited maximum current does flow through the regulator.

→ TO protect regulator, one method is used to limit the short circuit current and to allow higher current to the load such method is current foldback.



→ Voltage at C_L is divided by R3 - R4 n/w,

→ Transistor Q_2 conducts only when the

drop across R_{SC} is large enough to produced BE of $Q_2 = 0.5V$

→ This reduces the voltage V_1 at E of Q_1 E_1 output voltage V_O. The Base of Q_2 (C_L) will be $\frac{V_1 R_4}{R_3 + R_4}$

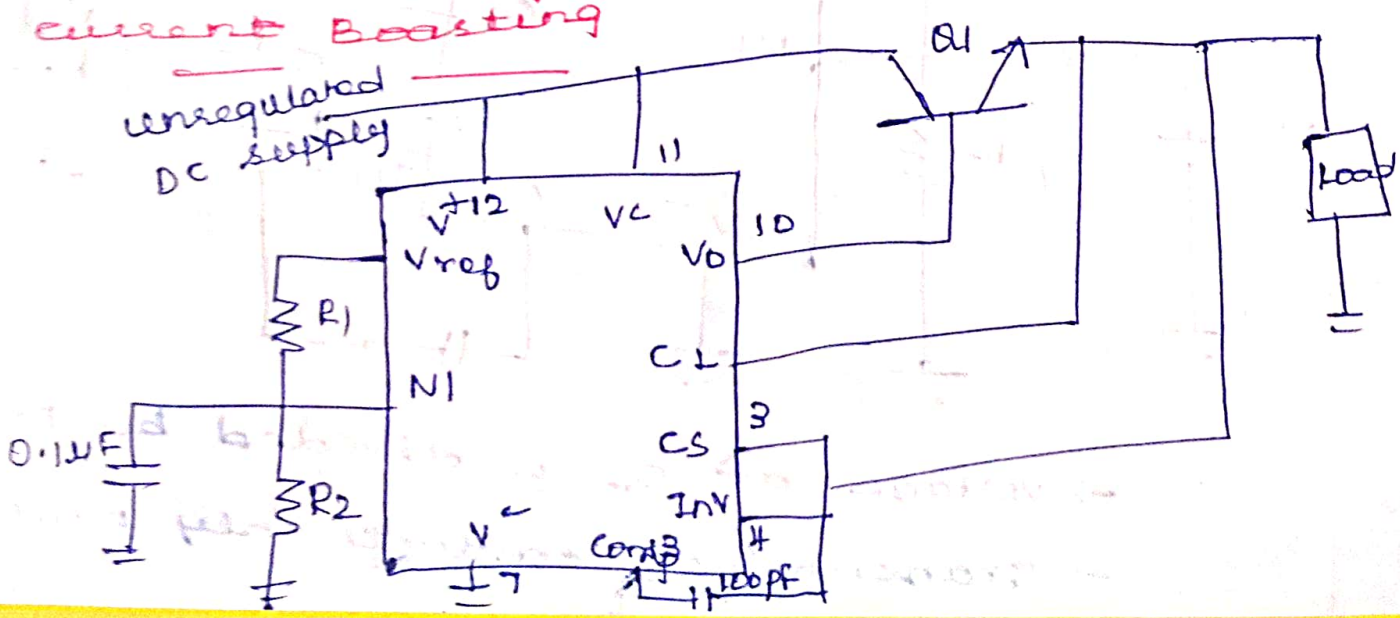
→ voltage at C_L drops by smaller amount compared to drop in voltage at E_S terminal.

→ Increasing the conduction of Q_2 which in turn reduces the conduction of Q_1 is I_1 further reduces.

→ It continues till $V_O = 0.V_1$ is just adjusted large to keep 0.5V between E_L E_1 C_S.

→ I_{SC} has been reduced by lowering both I_L and V_O.

Current Boosting



→ IC 723 regulator can provide maximum current is 140mA.

↳ for many applications, this is not sufficient.

→ It is possible to boost the current level simply by adding a boost transistor Q1 to the voltage regulator.

→ collector current of pass transistor Q1 comes from the unregulated dc supply.

→ output current from Vo drives the base of Q1.

↳ base current gets multiplied by the beta of the pass transistor.

$$I_{Load} = \beta I_B$$

LM 392 (power Amplifier)

→ high gain, internally frequency compensated operational amplifier and the other is a precision voltage comparator.

↳ Both the operational amplifier and the voltage comparator have been specifically designed to operate from a

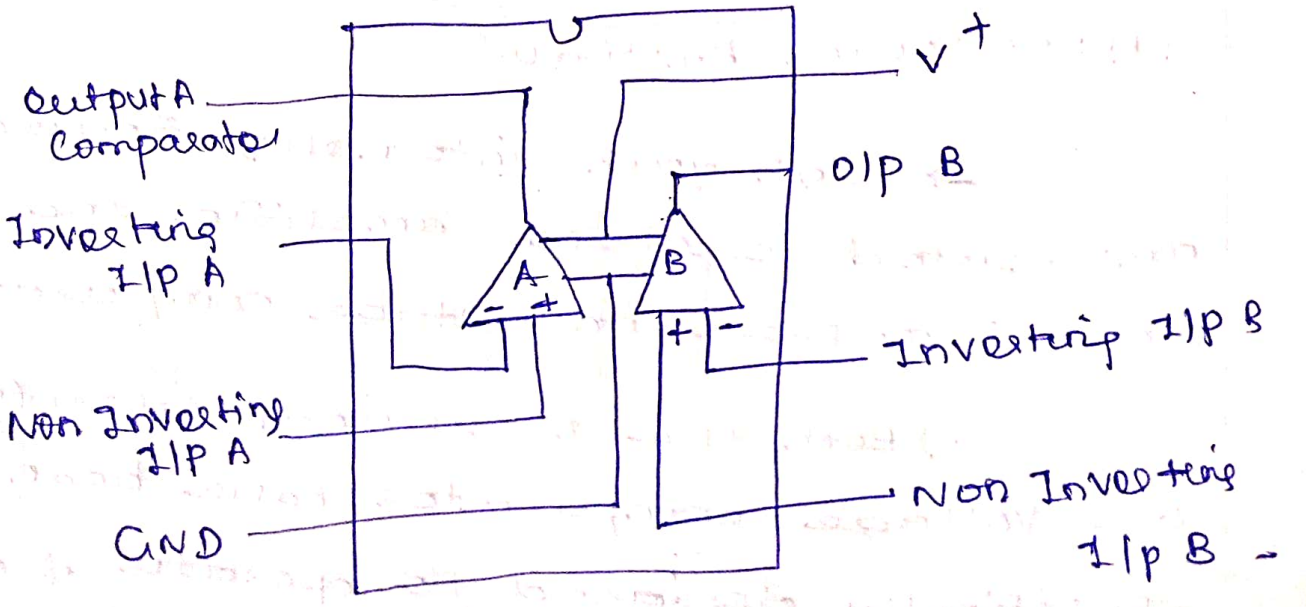
single power supply over a wide range of voltages.

↳ Both circuit have input stages which will common mode input down to ground when operating from a single power supply.

↳ operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Features

- → wide power supply voltage range
- → Low supply current drain.
- → Low input biasing current
- → Low input offset voltage
- → Low input offset current.



→ It consists of 2 independent building block circuits

↳ one is high gain, internally frequency compensated operational amplifier and other is a precision voltage comparator.

↳ Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages.

Application

→ Transducer amplifiers with pulse shaper

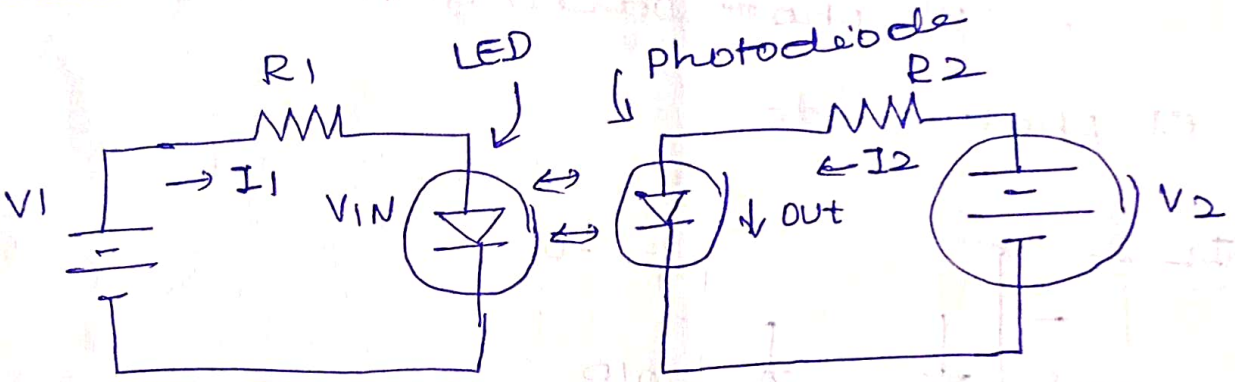
→ DC gain block with level detector

→ VCO as well as all conventional operational amplifier.

opto coupler :

→ optocoupler is a solid state complement in which the light emitter light path and light detector are all enclosed within the component and can't be changed from outside.

→ optocoupler provides electric isolation between two circuits.



→ source V_1, series Resistance R_1 decide the forward current I_1 through the LED

→ LED will emit light.

→ when the emitted light incident on photodiode, reverse current will set in the output circuit.

→ Due to the reverse current, voltage will be dropped across the resistor R_2.

$$V_o = V_2 - I_2 R_2$$

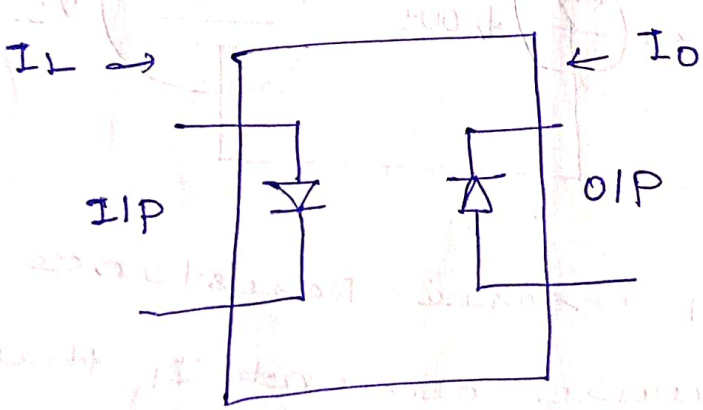
→ If input is changed, the amount of light emitted by LED will change. This will change the output voltage.

Types

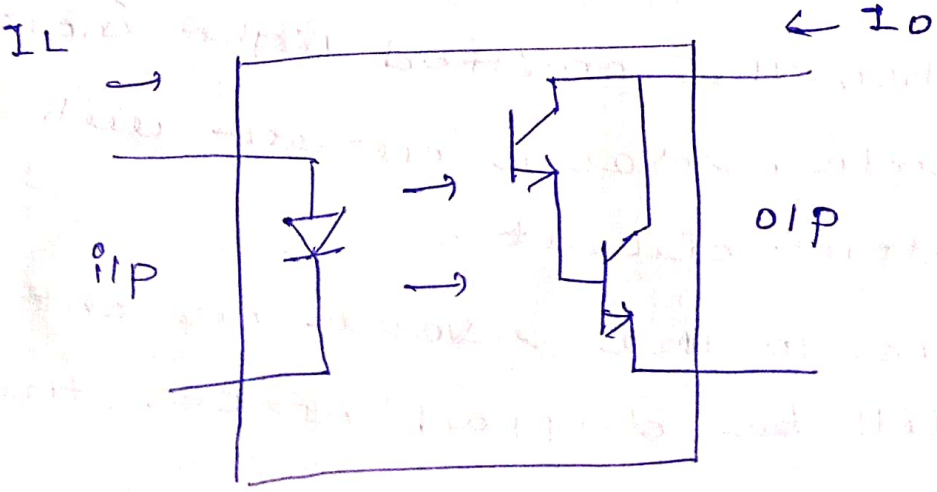
→ LED photodiode

→ LED photo Darlington.

LED photodiode



LED photo Darlington



Characteristics of opto coupler.

Current Transfer Ratio (CTR)

$$CTR = \frac{I_C}{I_F} \times 100\ \%$$

Isolation Voltage between I/p and O/p.

Isolation Voltage is another factor in choosing a photo coupler. This is because, photo couplers are used for angle transmission between circuits that have different potential, which tend to generate impulsive voltage.

Response time:

depends on

→ output photo transistor

→ Input forward current

→ Load resistance.

Bandwidth

20KHz – 500KHz

$I_{L(max)}$

max permissible dc current =

40mA – 100mA.

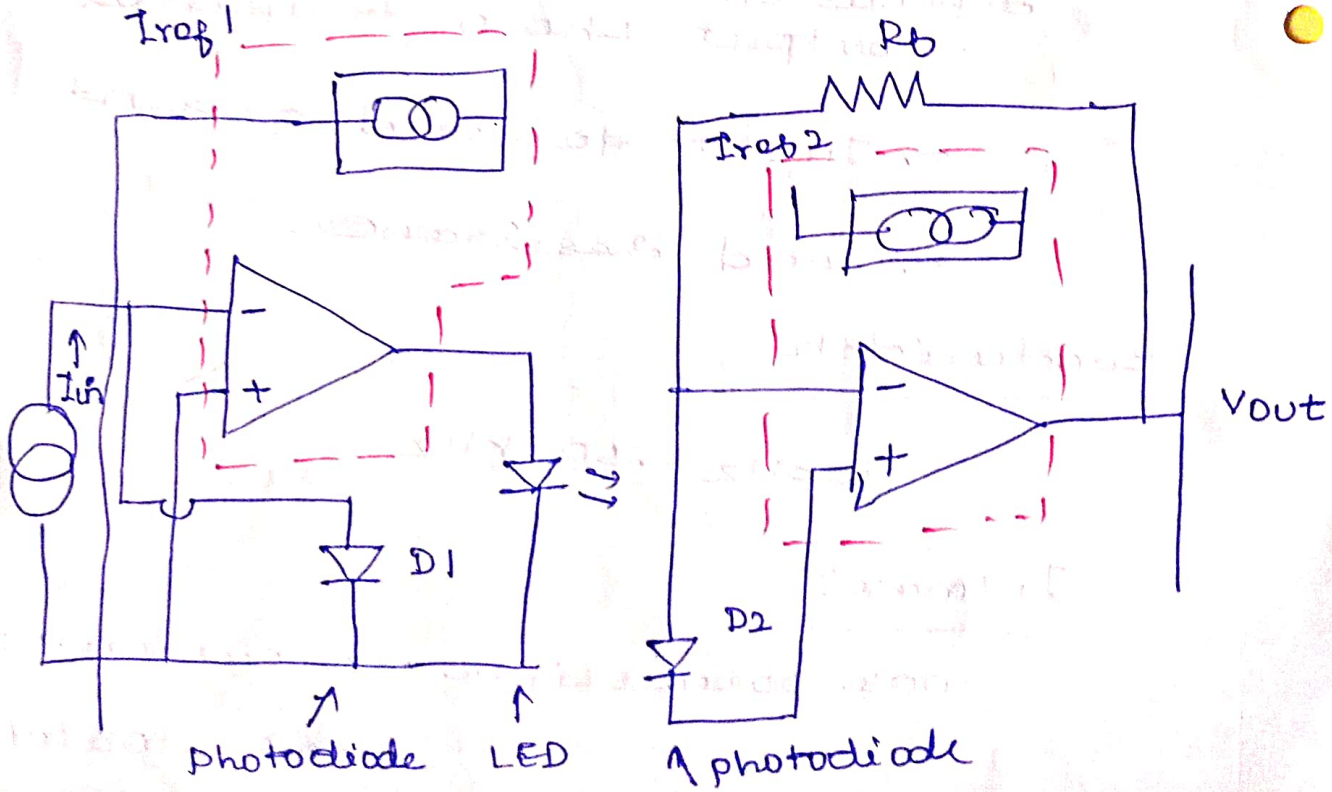
$V_{CE(max)}$:

maximum allowable dc voltage that can be applied to output photodiode.

Isolation amplifier

→ Isolation amplifier is an amplifier that offers an electrical isolation between its input and output terminals.

→ They can provide voltage difference of several thousands of volts between input and output.



→ LED and a pair of photodiode are coupled together to isolate the output signal from the input.

→ LED and photo diode are arranged such that some amount of light falls on each photo diode.

→ I_{ref1} and I_{ref2} are required to generate a midscale reference.

→ Negative feedback around A1 occurs through optical path formed by the LED and D1.

→ signal is transferred across the isolation barrier by the matched light path to D2.

→ LED light output increases, D1 responds by generating an increased current.

→ The current increases until the sum of currents in and out of the input node is zero.

→ At that point, negative feedback through D1 has stabilized the

loop.

$I_{D1} = I_{IN}$

$\therefore$ D_1 and D_2 are matched ($I_{D1} = I_{D2}$)

$I_{D2} \simeq I_{IN}$

→ current produced by D_2 must either flow into A_2.

→ A_2 is designed for low bias current almost all the current will flow through RF.

$$V_o = I_{D2} R_F \simeq I_{IN} R_F$$

Features

→ wide Bandwidth = 60kHz

→ 750V continuous isolation voltage.

→ Ultra low leakage : 0.3 μA, max at 240V/60HZ.

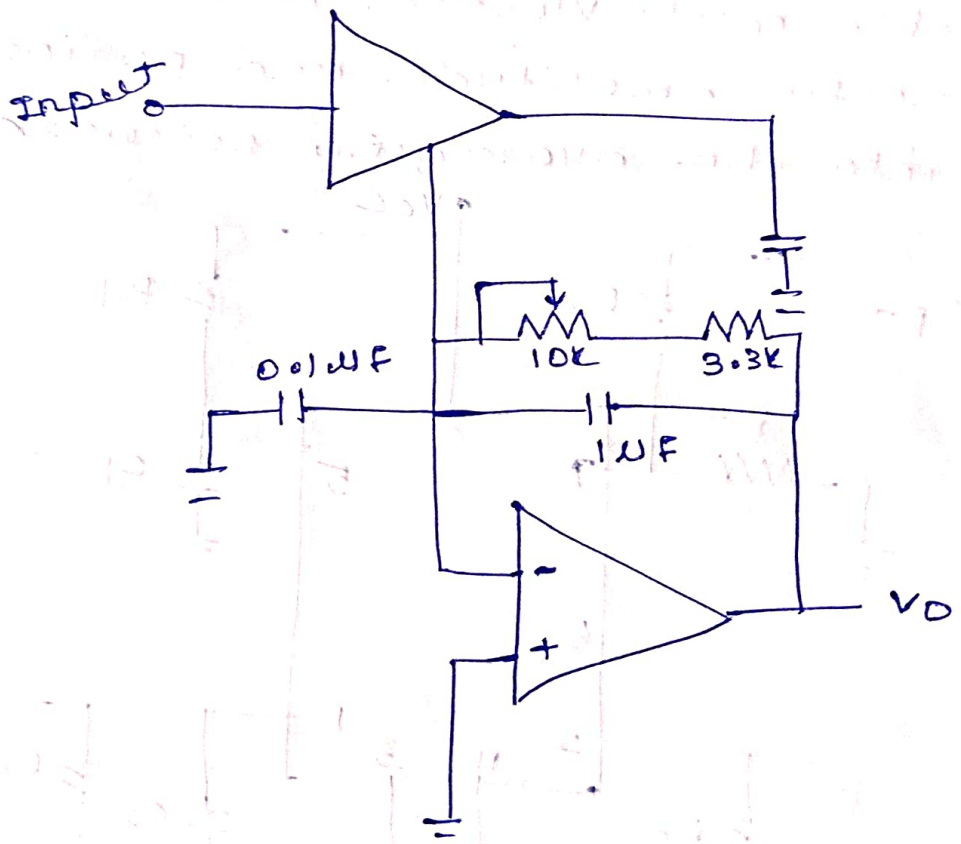
→ 18 pin DIP package.

Frequency to voltage and voltage to frequency converters

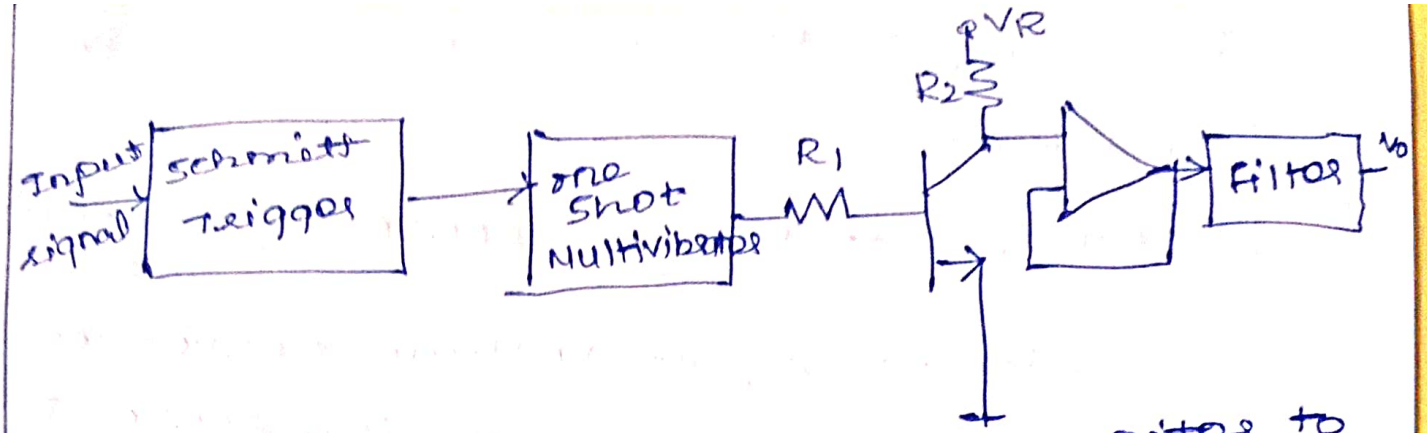
Frequency to voltage convertor circuits

→ Frequency to voltage convertor is an electronic device which converts the sinusoidal input frequency into a proportional current.

→ The basic circuit includes operational amplifier and RC circuits.



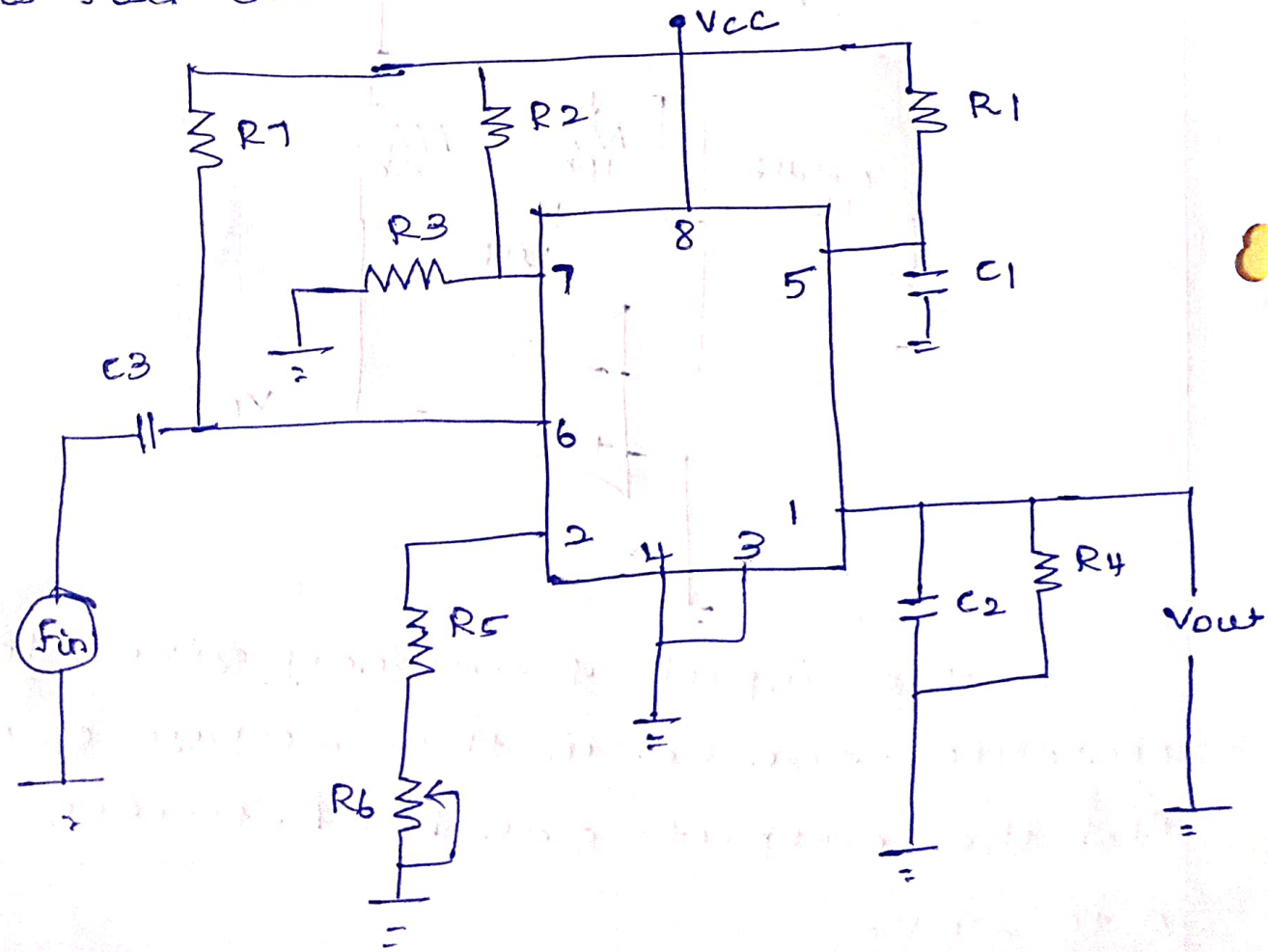
→ The input frequency given to this convertor can be in the range of 0-10kHz. And the output can be between 0 to -10V.



→ The circuit charges the capacitor to a certain level.

→ An Integrator is connected in it and the capacitor discharges into this integrator.

→ The precision switch and the monostable multivibrator generate a pulse of a specific amplitude and period which is fed into the averaging network.



F-V convertor working

→ The voltage on the output is proportional to the frequency at the input.

→ The timer circuit gets triggered by the built in comparator circuit in the IC when the negative edge of the pulse train.

→ The current flowing is proportional to the values of C1 and R1 and the input frequency.

→ The output voltage across the resistor RH which is proportional to the frequency of the input.

→ 15V DC is used in this circuit but the operating voltage of IC can be between 5V to 30V DC.

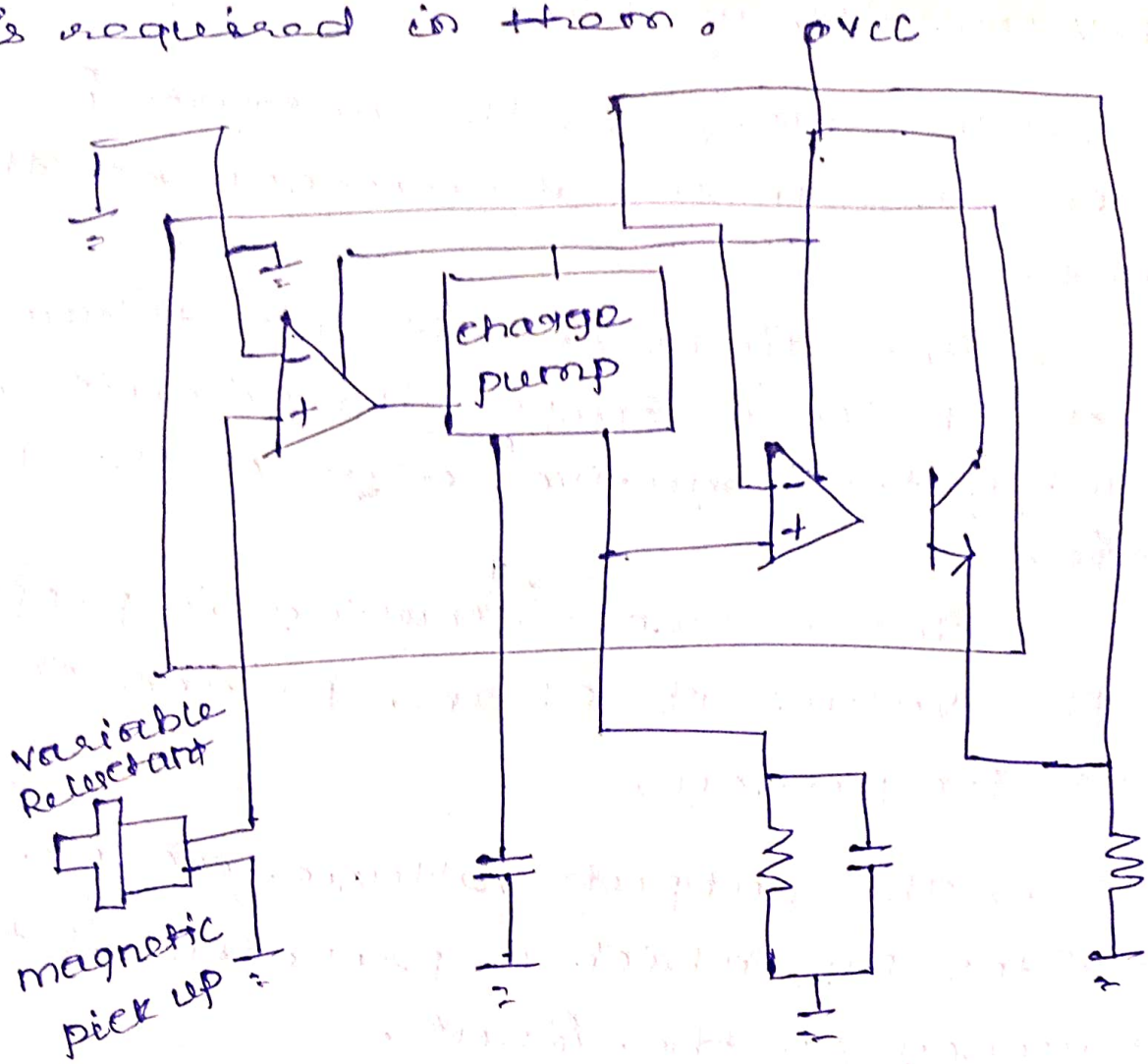
→ The value of the R3 is dependent upon the supply voltage.

F|V and Digital Tachometer:

→ A digital tachometer is an electronic device which measures the rate of rotation of a wheel.

→ They display the rate of rotation in the form of voltage which is why a frequency to voltage convertor

is required in them.



→ The rate of occurrence of some events can be measured by a rate meter.

→ It counts the events for a certain time period and then divides the no of events by the total time and hence we get a rate.

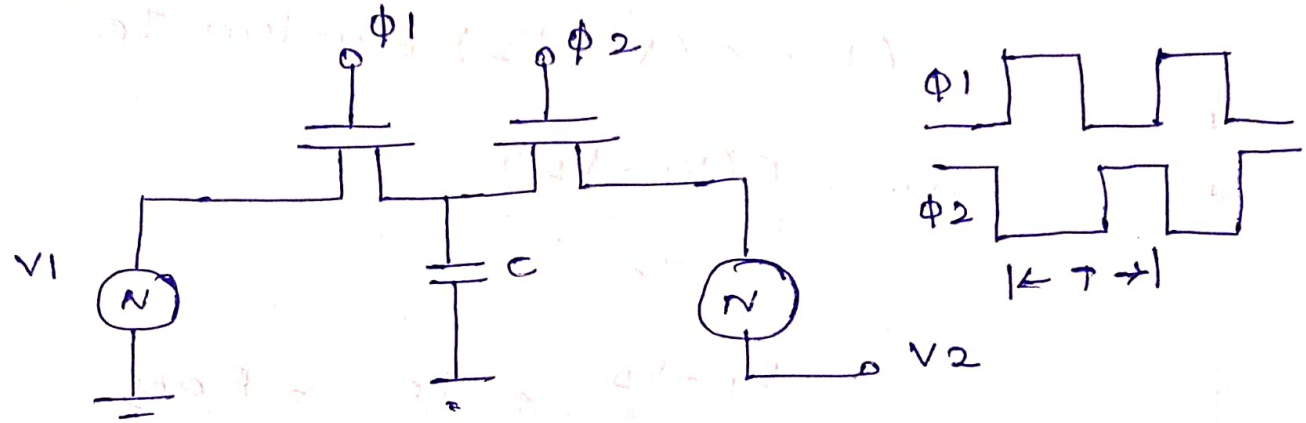
→ The capacitors C1 and C2 and the resistor R1 have specific values according to the circuit requirements

Switched capacitor Filters:

→ Large resistors in active RC filters are not practical in IC

↳ Large area

↳ Accurate control of R varies difficult.



→ circuit technique to solve the problem

↳ Replace resistors with capacitor

→ switches are usually realized with MOS switches having finite R, C

→ If $1/T_c >>$ frequency of interests, SW is acting as a resistor.

→ Assume initially ϕ_2 ON, ϕ_1 OFF and $V_1 > V_2$

$$Q = CV_2$$

→ when ϕ_2 is OFF and ϕ_1 is ON

$$Q = CV_1$$

$$\Delta Q = C(V_1 - V_2) \text{ supplied by } V_1$$

→ when ϕ_1 is OFF and ϕ_2 is ON

$$Q = CV_2$$

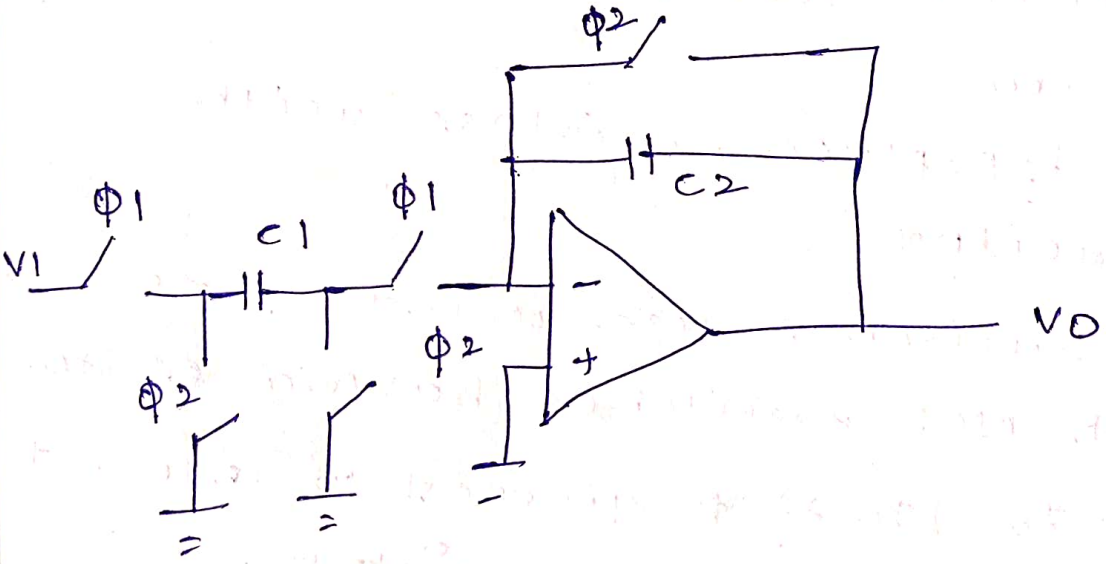
$\Delta Q = C(V_1 - V_2)$ supplied to V_2

→ switched capacitor deliver charges from V_1 to V_2

$\Delta Q = C(V_1 - V_2)$ during T_C

$$I_{avg} = \frac{C(V_1 - V_2)}{T_C}$$

$$\frac{V_1 - V_2}{I_{av}} = \frac{T_C}{C} = R_{eq}$$



Initially assume $Q_1, Q_2 = 0$

when ϕ_1 is ON, ϕ_2 is OFF

$$Q_1 = C_1 V_1$$

$$Q_2 = C_2 (0 - V_O)$$

But $Q_1 = Q_2$

$$C_1 V_1 = -C_2 V_O$$

$$V_o = -\frac{C_1}{C_2} V_i$$

During ϕ_1

$Q_1 = C_1 V_1$ $\quad Q_2 = 0$

During ϕ_2

$Q_1 = 0$ $\quad Q_2 = C_2 (V_o - 0)$

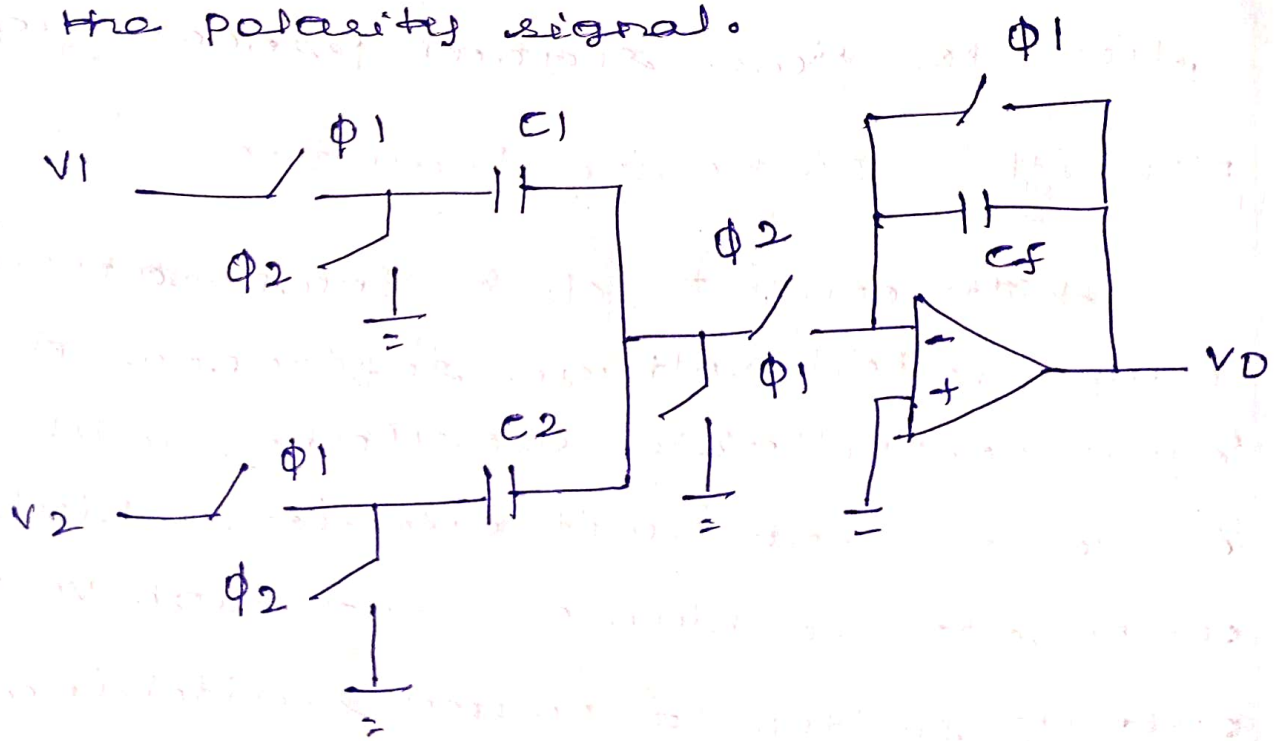
But $Q_1 = Q_2$

$C_1 V_i = C_2 V_o$

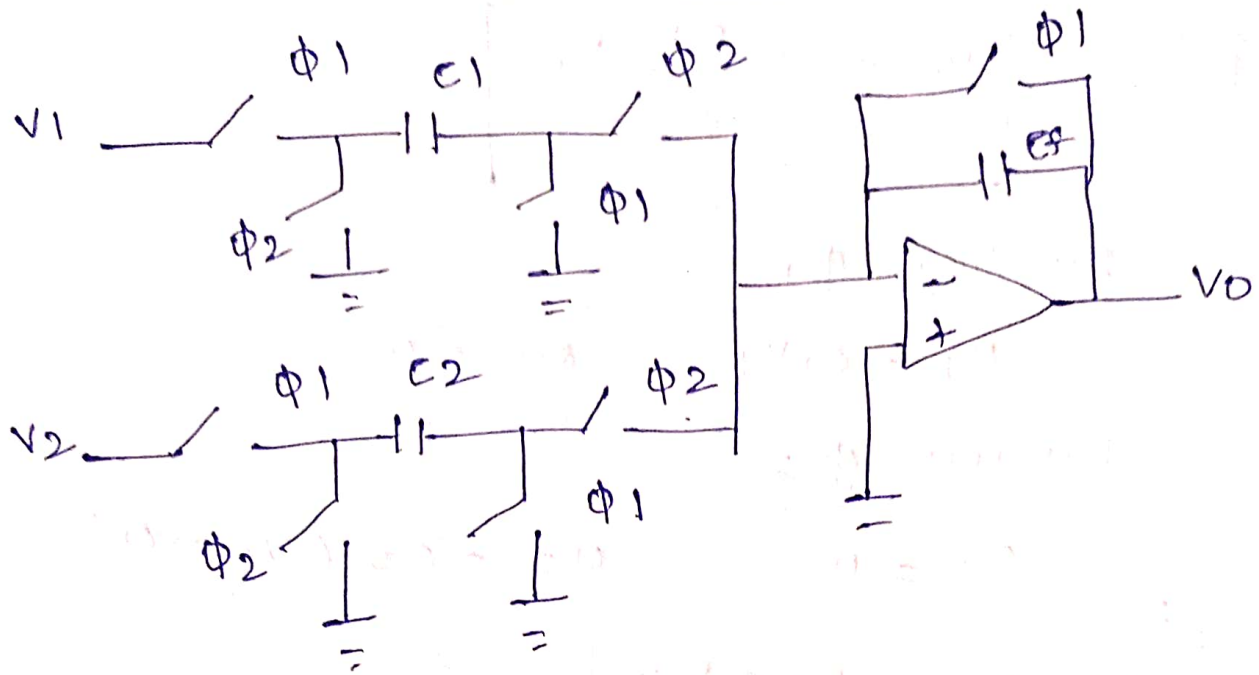
$$V_o = \frac{C_1}{C_2} V_i$$

→ Non Inverting Amplifier

by switching phase can change the polarity signal.



$$V_o = \left(\frac{C_1}{C_f} V_1 + \frac{C_2}{C_1} V_2 \right) V_i$$



$$V_0 = \left(\frac{C_1}{C_f} V_1 + \frac{C_2}{C_f} V_2 \right) V_1$$

→ SC filters perform discrete time domain signal processing.

↳ z domain analysis for discrete time signal processing.

Monolithic Switching Regulator:

→ It consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high current, high voltage output switch, a power switching diode and an uncommitted op-amp.

Feature:

→ step up, down & Inverting operation

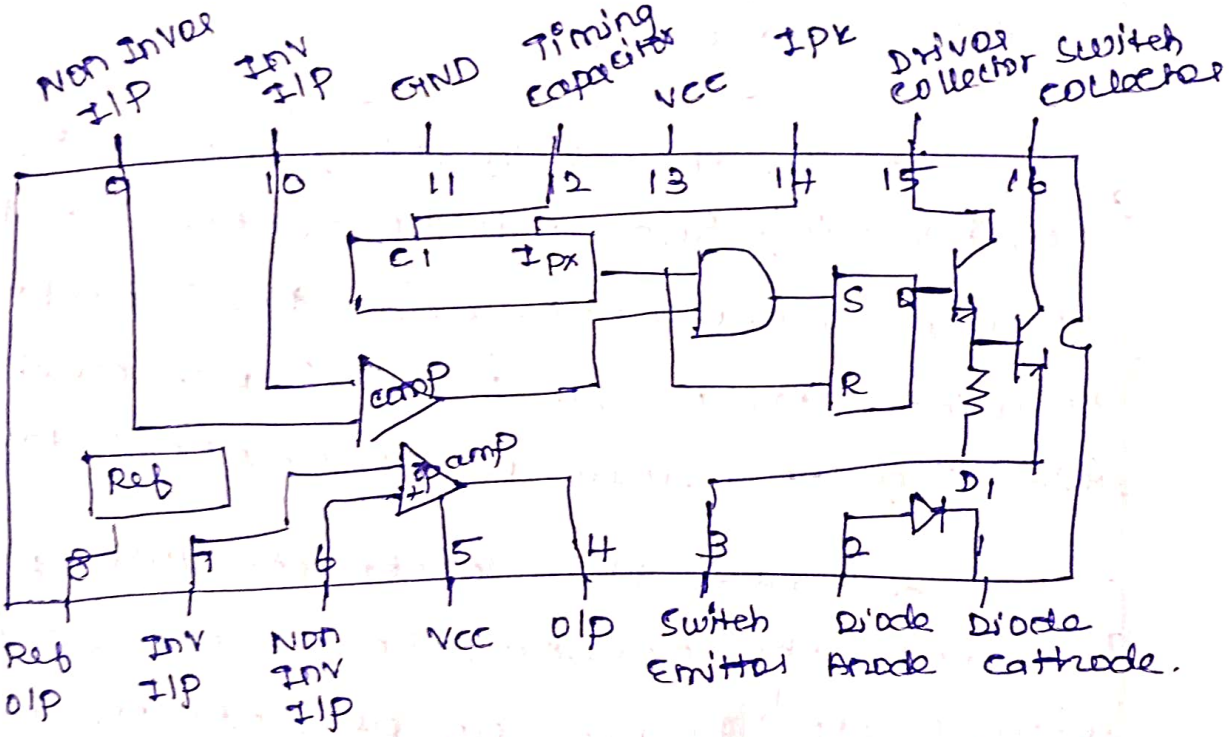
→ operation from 2.5 to 40V Input

→ 80 db line and load regulations.

→ output adjustable from 1.3 to 40V

→ peak current to 1.5A without external resistors.

→ Variable frequency, variable duty cycle device.



→ The internal switching frequency is set by the C1, connected between Pin 12 & Pin 11, the initial duty cycle is 6:1.

→ The switching frequency & duty cycle can be modified by the current

limit circuitry.

comparator:

→ The comparator modifies the OFF time of the output switch transistor Q1 & Q2.

→ In the step up & step down modes, the non inverting input of the comparator is connected to the voltage reference of 1.3V and the inverting input is connected to the output terminal via the voltage divides network.

→ In the inverting mode & the non inverting input is connected to both the voltage reference and the output terminal through 2 resistors and the inverting terminal is connected to ground.

→ When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.

→ If the output is too high & the voltage at the inverting terminal is higher than that at the non inverting terminal, then the comparator output goes low.