DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE (AUTONOMOUS)

PERAMBALUR - 621212

U23ECP31 –ELECTRONIC CIRCUITS AND DIGITAL LABORATORY

MANUAL

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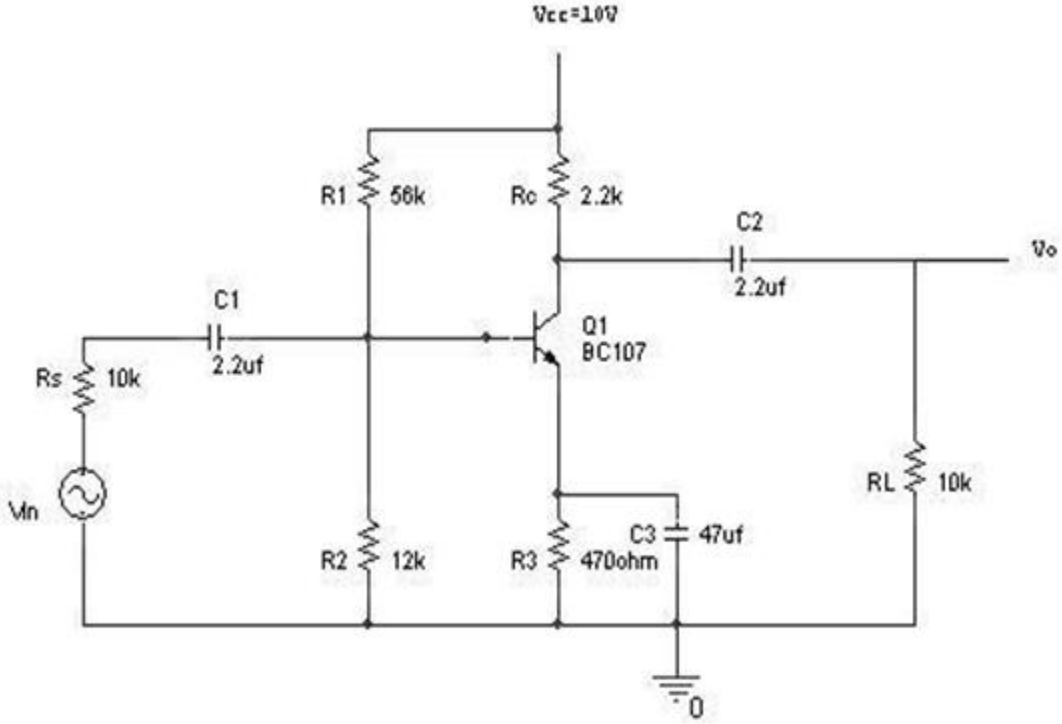
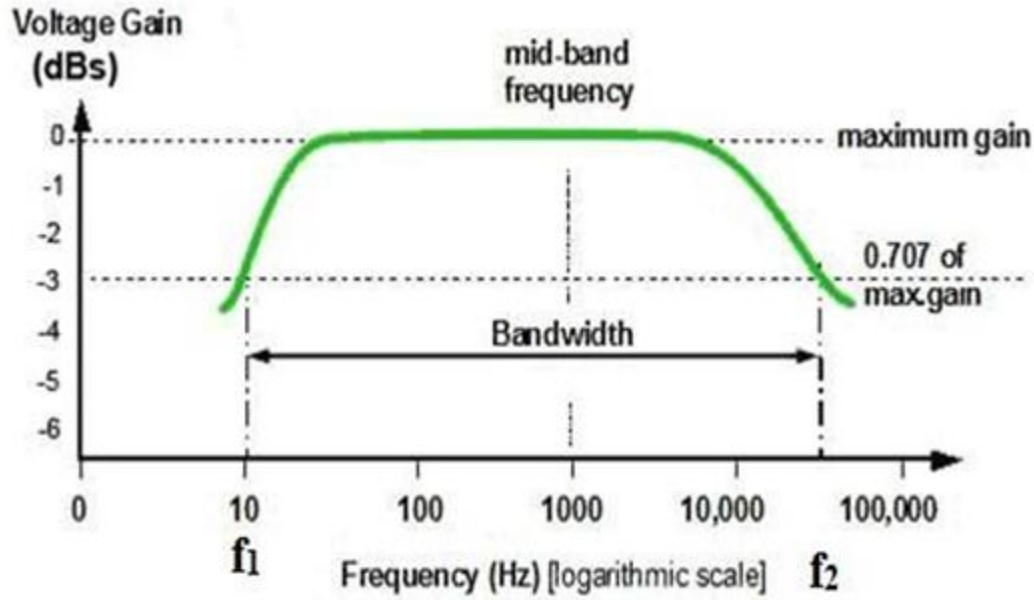
LIST OF EXPERIMENTS

1. Frequency Response of CE amplifier
2. Differential Amplifiers - Transfer characteristics, CMRR Measurement
3. Non-sinusoidal Waveform generators and converters (Astable & Monostable)
4. Design of Integrator and Differentiator
5. Analysis of FET, MOSFET with Fixed Bias, self-bias and voltage divider bias using simulation software
6. Design of RC Phase Shift Oscillator, Colpitt and Wien Bridge Oscillator using simulation software
7. Design of Half Adder and Full Adder using basic gates
8. Design of Multiplexer and De-multiplexer using logic gates
9. Design of code converters using logic gates (Binary to gray and vice-versa)
10. Design of Synchronous ripple counters

COMMON EMITTER AMPLIFIER CIRCUIT DIAGRAM:



MODEL GRAPH:



Band Width (BW) = $f_2 - f_1$

Exp.No:1. FREQUENCY RESPONSE OF COMMON EMITTER (CE) AMPLIFIER

DATE:

AIM:

To construct a Common Emitter Amplifier Circuit and to plot its frequency response characteristics

REQUIREMENTS:

S.NO	NAME OF THE APPARATUS/COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Audio Frequency Oscillator(AFO)	1MHz	1
2.	Dual DC Regulated Power Supply (RPS)	(0-30)V	1
3.	Cathode Ray Oscilloscope(CRO)	(0-30) MHz	1
4.	Connecting Wires	As necessary	
COMPONENTS REQUIRED			
4.	Transistor	BC107	1
5.	Resistor	56KΩ,12KΩ, 470Ω, 2.2KΩ, 10K Ω	1, 1, 1, 1, 2
6.	Capacitor	47μF, 2.2μF	1, 2
7.	CRO Probes	-	2
8.	Bread board	-	1

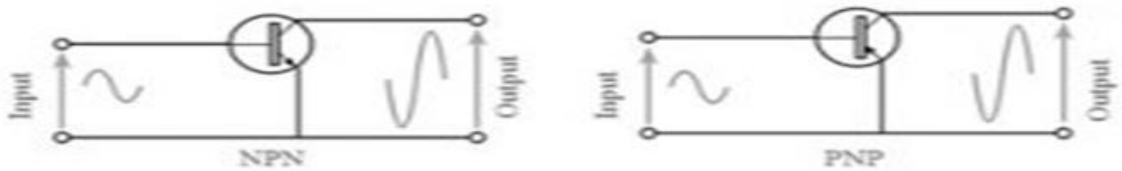
THEORY:

The Common Emitter Amplifier is a three basic single-stage bipolar junction transistor and is used as a voltage amplifier. The input of this amplifier is taken from the base terminal, the output is collected from the collector terminal and the emitter terminal is common for both the terminals. The configuration of a common emitter transistor is widely used in most electronic circuit designs. This configuration is evenly appropriate to both the transistors like PNP and NPN transistors but NPN transistors are most frequently used due to the widespread use of these transistors. In Common Emitter Amplifier Configuration, the Emitter of a BJT is common to both the input and output signal as shown below. The arrangement is the same for a PNP transistor, but bias will be opposite w.r.t NPN transistor.

Tabulation:

V_{in} = _______V

S. No	Input Signal Frequency in Hz	Output Voltage (V_o) in Volts	Gain in dB = 20 log (V_o / V_{in})



PROCEDURE

1. Connect the circuit as shown in the circuit diagram.
2. Apply an input of 50mV peak-to-peak and 10Hz frequency using function generator.
3. Measure the output voltage V_o (p-p) for various values of frequencies.
4. Tabulate the readings in the tabular column.
5. The voltage gain can be calculated by using the expression 20*log (V_0/V_i) in dB.
6. For plotting the frequency response the input voltage is kept constant at 50 V peak-to-peak and the frequency is varied from 10Hzto 2MHz using function generator
7. Note down the value of output voltage for each frequency.
8. All the readings are tabulated and voltage gain in dB is calculated by using the expression $20\log_{10}(V_0/V_{in})$
9. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis on a semi-log graph.
10. The bandwidth is calculated from the frequency response graph as $BW=f_2-f_1$.

RESULT:

Thus the Common Emitter Amplifier circuit is constructed and its frequency response is plotted.

- Lower cut off frequency (f_1)=-------------
- Upper cut off frequency (f_2)=-------------
- Bandwidth (BW)=--------------

VIVA QUESTIONS WITH ANSWERS

1. **What is a transistor?**

   A transistor is a three-terminal semiconductor device which is mainly used to amplify or change the direction of electronic signals.

2. **Who invented the transistor?**

   Walter Brattain, John Bardeen, and William Shockley invented the transistor.

3. **Where are transistors used?**

   Transistors are used in oscillators, amplifiers, and switches.

4. **What are the two types of transistors?**

   The two types of transistors are

   Bipolar Junction Transistors (BJT)

   Field Effect Transistors (FET)

5. **Define bipolar junction transistors.**

   A bipolar junction transistor is a semiconductor three-terminal device which features two P-N junctions and is able to amplify or magnify electrical signals.

6. **What is an NPN transistor?**

   NPN transistor is a type of transistor in which a p-type semiconductor is sandwiched between two p-type semiconductors. In NPN transistors, electrons are the majority charge carriers, and holes are the minority charge carriers.

7. **What is a PNP transistor?**

   PNP transistor is a bipolar junction transistor formed with three layers of semiconductor material, with two P-type regions and one N-type region.

8. **What is the equation for voltage gain?**

$$A_\text{v} \triangleq \frac{v_\text{out}}{v_\text{in}} = \frac{-g_m R_\text{C}}{g_m R_\text{E} + 1} \approx -\frac{R_\text{C}}{R_\text{E}} \qquad (\text{where} \quad g_m R_\text{E} \gg 1).$$

9. **What is cut off frequency?**

   In electronics, cutoff frequency or corner frequency is the frequency either above or below which the power output of a circuit, such as a line, amplifier, or electronic filter has fallen to a given proportion of the power in the pass band.

10. **What is lower 3dB and upper 3dB cut off frequency?**

Most frequently this proportion is one half the pass band power, also referred to as the 3 dB point since a fall of 3 dB corresponds approximately to half power. As a voltage ratio this is a fall to the pass band voltage

11. **What are the applications of CE amplifier?**

Low frequency voltage amplifier, radio frequency circuits and low-noise amplifiers

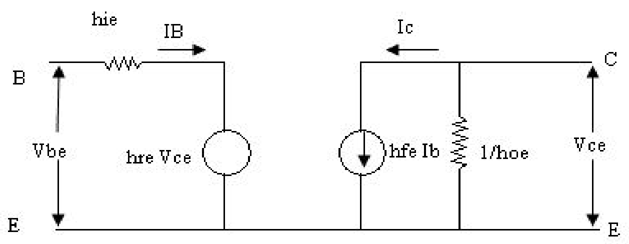
12. **What is Bandwidth of an amplifier?**

Bandwidth is the difference between the upper and lower frequencies in a continuous set of frequencies. It is typically measured in hertz.

13. **What is the importance of gain bandwidth product?**

This quantity is commonly specified for operational amplifiers, and allows circuit designers to determine the maximum gain that can be extracted from the device for a given frequency.

14. **Draw h parameter equivalent circuit of CE amplifier.**



15. **What is the importance of coupling capacitors in CE amplifier?**

Input coupling capacitor couples the signal to base of the transistor, it blocks any DC component present the signal and passes only a.c signal for amplification. Output coupling capacitor couples the output signal to the load or to the next stage of the amplifier, it blocks any DC component present the signal and passes only ac part of the amplified signal.

16. **What is the importance of emitter by pass capacitor?**

Emitter bypass capacitor provide a low reactance path to the amplified ac signal, if it is not connected in parallel with RE, the amplified ac signal passing through RE will cause more voltage drop across it.

17. **What type of feedback is used in CE amplifier?**

Negative feedback is used in CE amplifier.

18. **Why frequency response of the amplifier is drawn on semi-log scale graph?**

The frequency response of a given frequency dependent circuit can be displayed as a graphical sketch of magnitude (gain) against frequency (f). The horizontal frequency axis is usually plotted on a logarithmic scale while the vertical axis representing the voltage output or gain, is usually drawn as a linear scale in decimal divisions. Since a systems gain can be either positive or negative, the y-axis can therefore have both positive and negative values.

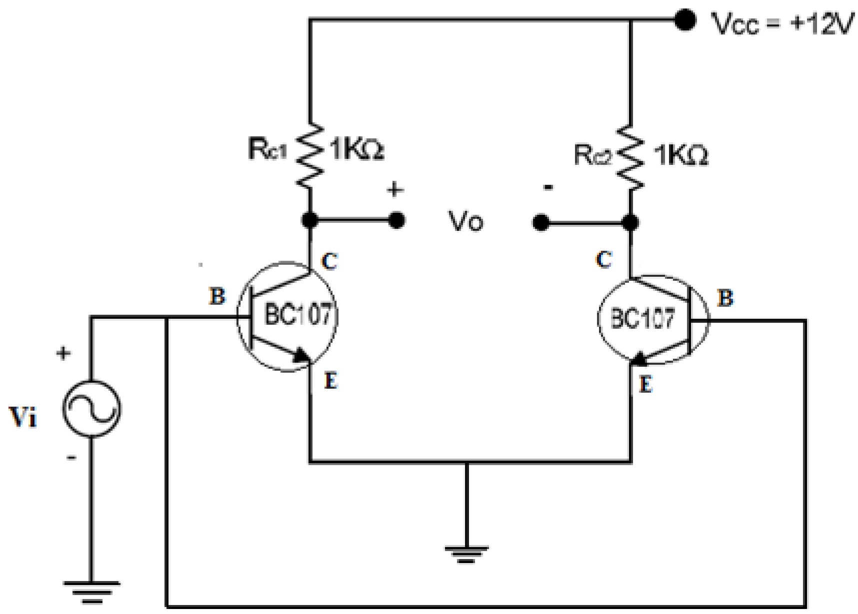
19. **If Q point is not properly selected, then what will be the effect on the output waveform?**

If the Q-point is not properly selected, we won't get the faithful amplification at output.The output will be clipped off at the positive peak or at the negative peak.

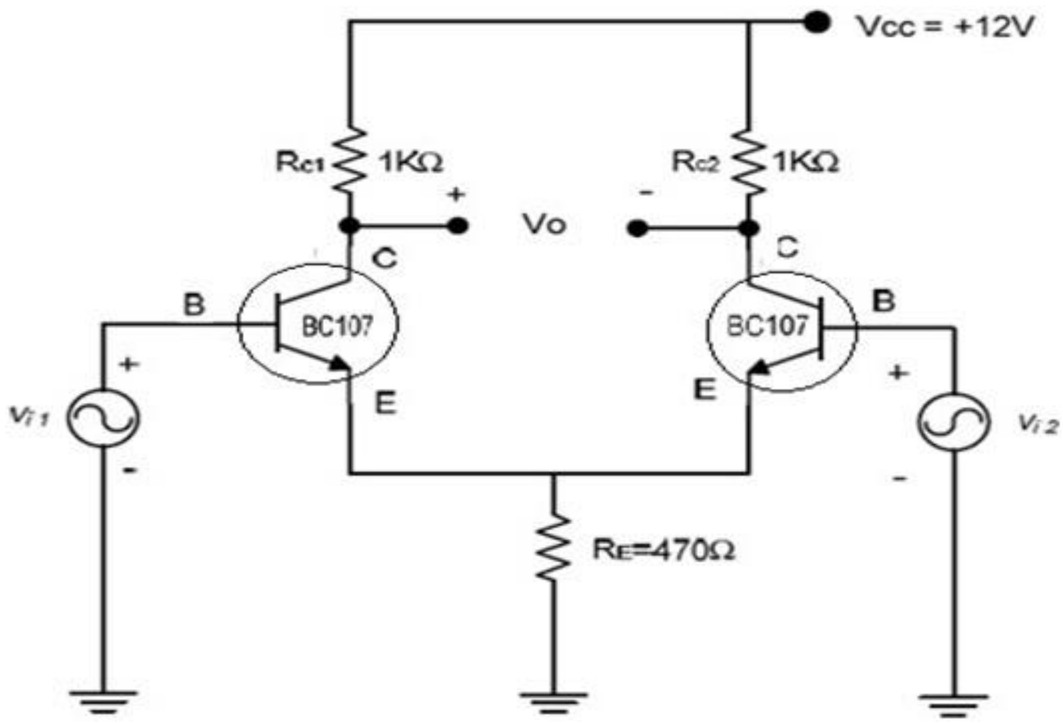
20. **What are the typical values of the input impedance and output impendence of CE amplifier?**

The input impedance is in the order of 1Kohm and the output impedance is in the order of 40Kohms.

CIRCUIT DIAGRAM: For Common mode Differential Amplifier:



CIRCUIT DIAGRAM: For Differential mode Differential Amplifier:



Exp.No:2. DIFFERENTIAL AMPLIFIERS - TRANSFER CHARACTERISTICS, CMRR MEASUREMET

DATE:

AIM:

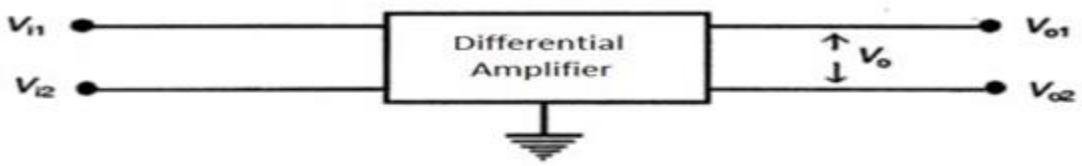
To construct a differential amplifier circuit and to find the difference mode gain, common Mode gain, Common Mode Rejection Ratio and also find its transfer characteristics.

REQUIREMENTS:

S.NO	NAME OF THE APPARATUS/COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Audio Frequency Oscillator(AFO)	(0-3)MHz	1
2.	Dual DC Regulated Power Supply (RPS)	(0-30)V	1
3.	Cathode Ray Oscilloscope(CRO)	(0-30) MHz	1
4.	Connecting Wires	As necessary	
COMPONENTS REQUIRED			
4.	Transistor	BC107	2
5.	Resistor	1KΩ,470Ω	2,1
6.	Probes	-	2
7.	Bread board	-	1

THEORY:

The amplifier which amplifies the difference between two input signals is called as Differential amplifier. The differential amplifier configuration is very much popular and it is used in variety of analog circuits. As the name indicates Differential Amplifier is a dc-coupled amplifier that amplifies the difference between two input signals. It is the building block of analog integrated circuits and operational amplifiers (op-amp). One of the important features of differential amplifier is that it tends to reject or nullify the part of input signals which is common to both inputs. This provides very good noise immunity in a lot of applications. Let's see the block diagram of a differential amplifier.



Differential Amplifier

V_{i1} and V_{i2} are input terminals and V_{o1} and V_{o2} are output terminals with respect to ground. We can feed two input signals at the same time or one at a time. In the former case it is called dual input otherwise it is single input. Similarly there are two ways to take output also. If the output is taken from one terminal with respect to ground, it is unbalanced output or if the output is taken between two output terminals, it is balanced output.

PROCEDURE

1. Check the equipment and components to ensure their proper working condition.
2. To Calculate common mode gain,

   i. Connect the circuit as shown in figure using bread board with very short wires.

   ii. Set the input using signal generator with the help of CRO.

   iii. Switch ON the power supply.

   iv. Measure the output voltage V_{01} by connecting the probe between collector-1 and ground and measure V_{02} by connecting the probe between collector-2 and ground using the two channels of the CRO and tabulate it on the table.

   v. Calculate the common mode gain using the given formulae.

   vi. After completion of the experiment, reduce the power to zero position and disconnect the circuit.

3. To Calculate differential mode gain,

   i. Connect the circuit as shown in figure using bread board with very short wires.

   ii. Set the input using signal generator with the help of CRO.

   iii. Switch ON the power supply.

iv. Measure the output voltage V01 by connecting the probe between collector-1 and ground and measure V02 by connecting the probe between collector-2 and ground using the two channels of the CRO and tabulate it on the table.

v. Calculate the differential mode gain using the given formulae.

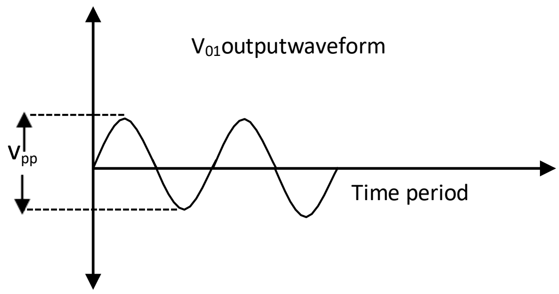
vi. After completion of the experiment, reduce the power to zero position and disconnect the circuit.

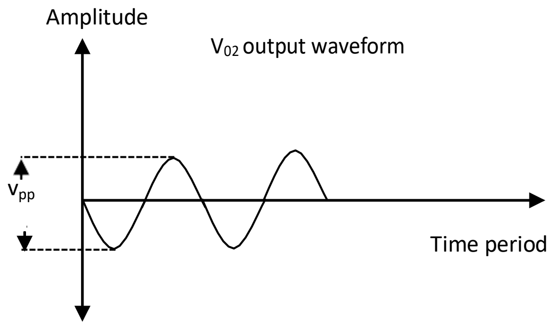
4. Calculate common mode rejection ratio (CMRR) using the difference mode gain and & common mode gain.

MODELGRAPH

i) For differential mode operation

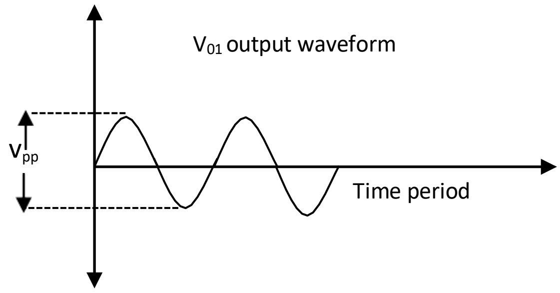
Amplitude



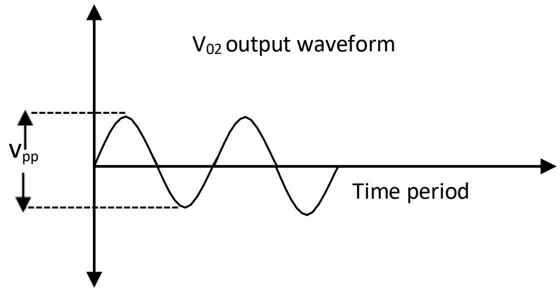


ii) For common mode operation

Amplitude



Amplitude



Tabulation:

(i) For Common Mode:

Input Voltages		Overall Input Voltage V_{ic} = (Vs1 + Vs2) / 2 (Volts)	Output Voltages V_{oc}(Volts)	Common Mode Gain in dB AC=20log(V_{0c}/V_{ic})
V_{s1}	V_{s2}			

(ii) For Differential Mode:

Input Voltages		Overall Input Voltage V_{id} = (V_{s2}- V_{s1}) (Volts)	Output Voltages V_{od}(Volts)	Common Mode Gain in dB AC=20log(V_{0d}/V_{id})
V_{s1}	V_{s2}			

FORMULAE USED:

1. Differential mode gain $A_d = V_{od}/ V_{id}$.

2. Common mode gain $A_C = V_{oc} / V_{ic}$.

V_{od}= ($V_{02} \sim V_{01}$) - Output voltage in differential mode operation.

V_{oc}= ($V_{02} \sim V_{01}$) - Output voltage in common mode operation.

For differential mode operation, the input voltage, $V_{id} = (V_{S2} – V_{S1})$ Volts

For common mode operation, input voltage is $V_{ic} = (V_{S1} + V_{S2}) / 2$ Volts

Where, V_{01} = output voltage at Q1.

V_{02}= output voltage at Q2.

V_{S1}= Input voltage to Q1.

V_{S2}= Input voltage to Q2.

3. Common Mode Rejection Ratio (CMRR) = Ad /Ac.

RESULT:

Thus the differential amplifier was successfully designed and constructed and the gain of the amplifier was found as follows.

i) Differential mode gain(A_d) in dB=---------------

ii) Common mode gain(Ac)in dB =---------------

Common mode rejection ratio = -------------

VIVA QUESTIONS WITH ANSWERS

1. What is differential amplifier?

Ans. An amplifier, which is designed to amplify the difference between two input signals, is called the differential amplifier. The differential amplifier is also referred to as a difference amplifier.

2. Advent of ICs made the differential amplifier extremely popular in both BJT and MOS technologies. Why?

Ans. The main requirements of differential amplifiers are matched devices and use of more components and IC fabrication is capable of providing matched devices and is also capable of providing large number of transistors at relatively low cost.

3. Why are differential amplifiers preferred over single ended amplifiers?

Ans. Basically there are two reasons for using differential amplifiers in preference to single ended amplifiers. First, the differential amplifiers are much less sensitive to noise and interference than single ended circuits. The second reason for preferring differential amplifiers is that the differential configuration enables us to bias the amplifier and to couple amplifier stages together without the necessity of bypass and coupling capacitors.

4. What is the basis of classification of differential amplifier configurations?

Ans. The differential amplifier configurations are classified on the basis of the number of inputs and the way an output voltage is measured.

5. What are differential configurations of differential amplifier?

Ans. The configurations are categorized on the basis of the number of inputs and the way an output voltage is measured. Accordingly, differential amplifier configurations may be classed as follows:

1. Dual-input, balanced-output differential amplifier configuration.
2. Dual-input, unbalanced-output differential amplifier
3. Single-input, balanced-output differential amplifier
4. Single-input. unbalanced-output differential amplifier

When both the inputs are used, the configuration is said to be dual input, otherwise single input. On the other hand, when the output voltage is measured between two collectors, it is referred to as a **balanced output**, because both collectors C_1 and C_2 are at the same dc potential w.r.t. ground. In case the output is measured across any one collector (either C_1 or C_2) w.r.t. ground, the configuration is known as an **unbalanced output**.

6. Which one of the four configurations is not commonly used and why?

Ans. Single-input, unbalanced-output differential amplifier configuration is rarely used because of the following two reasons:

1. This configuration is identical to the CE amplifier but it requires comparatively more components and provides less voltage gain than that of CE amplifier.
2. There exists a dc output voltage without any input signal applied.

7. What is difference between balanced and unbalanced output?

Ans. When the output voltage is measured between two collectors, the configuration is referred to as a balanced output, and if it is measured across any one collector (either C_1 or C_2) with respect to ground, the configuration is then said to be unbalanced output.

8. Why dc analysis of a differential amplifier circuit is required?

Ans. DC analysis of a differential amplifier circuit is required for determination of operating point (quiescent collector current I_{CQ} and quiescent collector-emitter voltage V_{CEQ}).

9. Why dc analysis made for dual-input, balanced-output differential amplifier configuration is also applicable for the remaining configurations too?

Ans. DC analysis for all the four configurations of the differential amplifiers is the same as long as same biasing arrangement is used for each of them.

10. Define CMRR.

Ans. CMRR is defined as the ratio of differential voltage gain to common-mode voltage gain and it is given by the equation

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

11. What are the advantages of differential amplifiers with swamping resistors?

Ans. The advantages of differential amplifiers with swamping resistors are as follows:

1. The dependence of the voltage gain of the differential amplifiers on variations in dynamic emitter resistance r'_e is reduced.
2. Linearity range of the differential amplifiers is increased.

12. What are the disadvantages of just increasing R_E for improving CMRR?

Ans. It is necessary that all the resistors are carefully ratio-matched so as to have excellent CMRR. The feedback connection for inverting and non-inverting amplifiers maintains the differential voltage v_d near zero volt. Increase in the value of emitter resistor R_E may cause permanent damage to the device.

13. Why R_E is replaced by a constant current source in a differential amplifier?

Ans. The resistor R_E in the differential amplifier is replaced by a constant current source in order to improve CMRR without affecting the operating point of the amplifier and without increasing the negative supply voltage $-V_{EE}$.

14. What is the current mirror?

Ans. The circuit in which the output current is forced to be equal to the input current is called current mirror circuit. Figure 2 shows block diagram and circuit diagram.

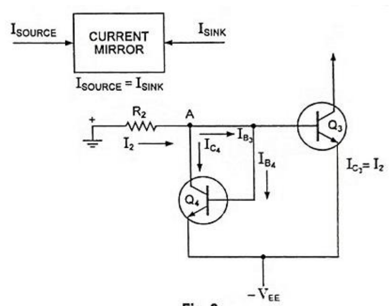


Fig. 2

15. What is the primary advantage of using an active load?

Ans. The differential voltage gain A_d is improved and as a result, the differential gain A_d is much higher with an active load than with an ordinary resistor.

16. Explain the advantages of active load over passive load.

Ans. Advantages of active load over passive load are as follows:

1. The differential voltage gain A_d is improved and as a result the differential gain A_d is much higher with an active load than with any ordinary resistor.
2. Active load takes less area than that taken by passive load on the chip in IC fabrication and, therefore, higher packing

17. Explain the difference between constant bias and current mirror?

Ans. The constant current bias is a circuit that provides current stabilization and therefore assures a stable operating point for the differential amplifier. The circuit in which output current is forced to be equal to be the input current is said to be a current mirror circuit. Thus, in current mirror the output current is a mirror image of input current. The current mirror is a special case of constant current bias and, therefore, can be used to provide constant current in different amplifier stages.

18. What is level translator?

Ans. Level translator circuit is usually an emitter follower circuit which is used to shift the dc level at the output of the intermediate stage downward to zero volt w.r.t. ground in a cascaded differential amplifier.

19.What is the main use of differential amplifier?

The purpose of the differential amplifier is to increase the amplitude of the heart signal to a level where it can be converted into a digital form. The gain of the circuit can be adjusted by appropriate selection of external resistors connected between the output and input terminals.

20.What is the gain of the differential amplifier transistor?

Gain of an amplifier is defined as V_{OUT}/V_{IN}. For the special case of a differential amplifier, the input V_{IN} is the difference between its two input terminals, which is equal to (V_1-V_2) as shown in the following diagram. Gain = $V_{OUT}/(V_1-V_2)$.

Exp.No:3.A) NON-SINUSOIDAL WAVEFORM GENERATORS AND CONVERTERS (ASTABLE)

DATE:

AIM:

To construct a transistor Astable multivibrator circuit for 1 KHz and (i) plot the collector and base waveforms (ii) measure the frequency of oscillation.

REQUIREMENTS:

S.NO	NAME OF THE APPARATUS /COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Audio Frequency Oscillator(AFO)	(0-3)MHz	1
2.	Dual DC Regulated Power Supply	10V	1
3.	Cathode Ray Oscilloscope(CRO)	(0-30) MHz	1
4.	Connecting Wires	As necessary	
5.	Multimeter	1	
COMPONENTS REQUIRED			
6.	Transistor	BC548	2
7.	Resistors	2.2KΩ,75KΩ	Each2
8.	Capacitors	0.01μF	2
9.	Probes	-	2
10.	Bread board	-	1

THEORY:

Multivibrator is considered as a non-sinusoidal oscillator which can generate waveforms other than sine wave. They are basically two-stage amplifiers with positive feedback from the output of one amplifier to the input of the other. This feedback is supplied in such a manner that one transistor is driven to saturation (ON state) and other to cut-off (OFF state). The action is reversed after a certain time, depending upon the circuit conditions i.e., the saturated transistor is driven into cut-off and the cut-off transistor is driven into saturation.

There are three basic types of multivibrators.

1. Astable multivibrator
2. Monostable multivibrator
3. Bistable multivibrator

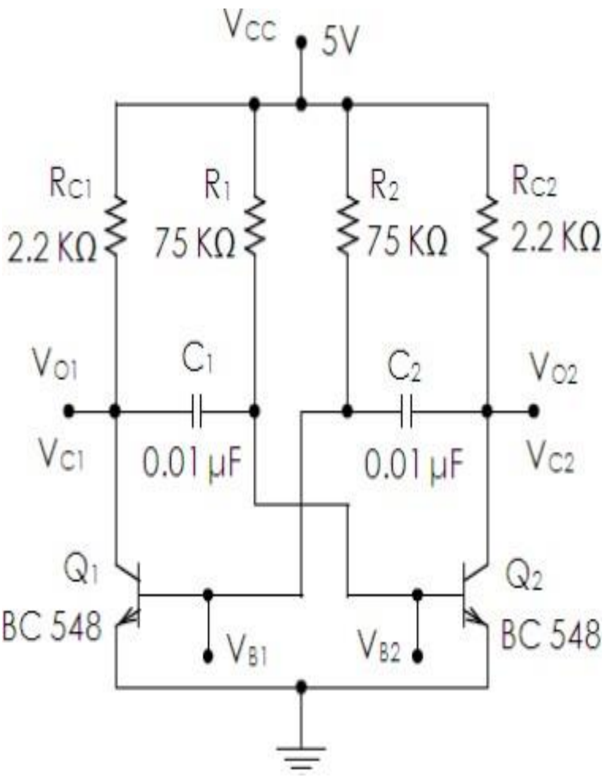
Astable multivibrator

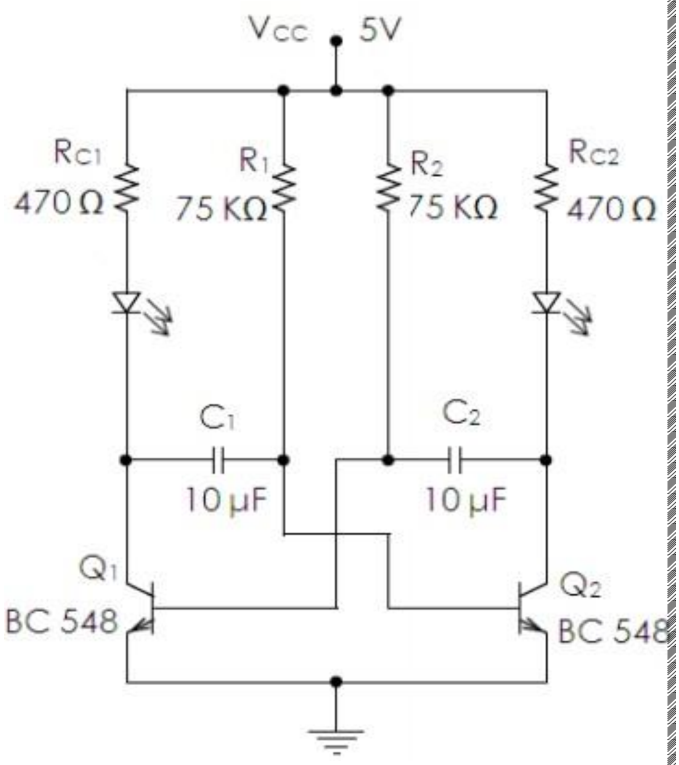
It is also called free-running relaxation oscillator. It has no stable state but only two quasi-stable states between which it keeps oscillating continuously of its own accord without any external excitation. When one transistor is in ON state and other remains in OFF state. Both will not be in same state at the same time.

PROCEDURE:

1. Check the given components
2. Assemble the circuit on a bread board
3. Switch ON the power supply
4. Connect the output to oscilloscope
5. Observe the waveforms at relevant points in the circuit
6. Measure the amplitudes and time periods and plot these waveforms
7. Assemble the second circuit and visually verify the output

CIRCUIT DIAGRAM: ASTABLE MULTIVIBRATOR

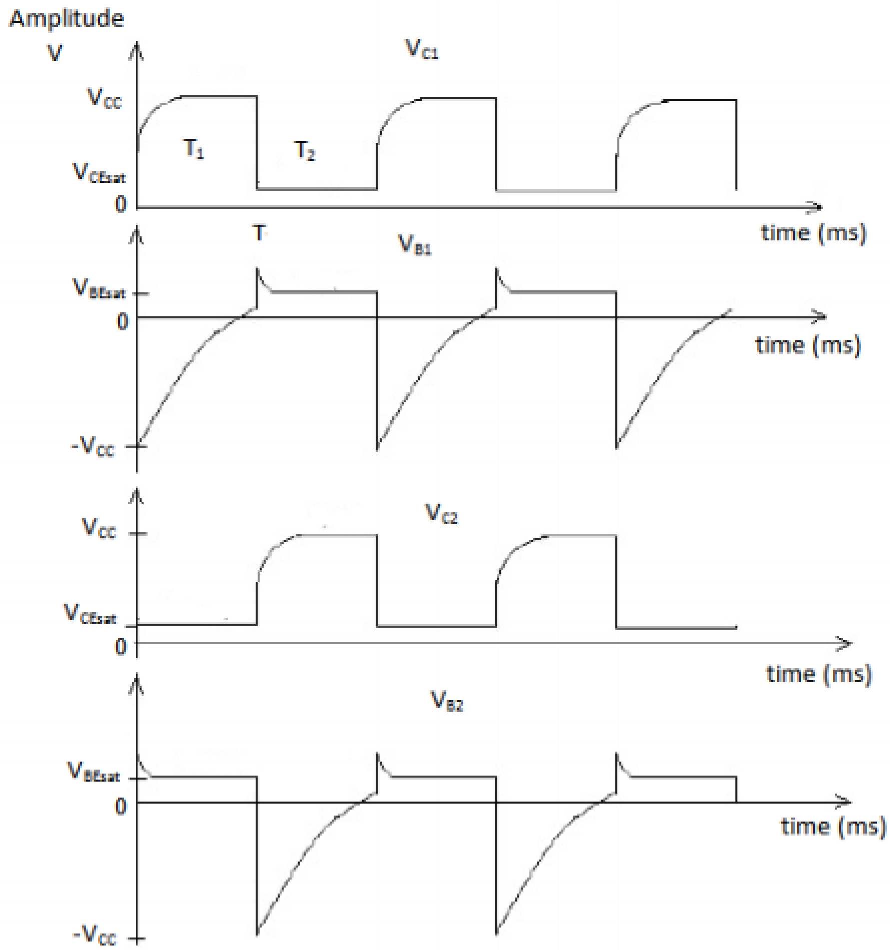




DESIGN

1. For 1 KHz frequency:
   $T_{OFFQ}2$ = 0.693 R C = 0.693 x 75 x 10^3 x C = 0.5ms
   C = 0.01μF
   T_{OFFQ1} = 0.693 R C = 0.693 x 75 x 10^3 x C = 0.5ms
   C = 0.01μF T = 1ms, f = 1/T= 1 KHz

MODEL GRAPH:



TABULATION:

ON time of Q1, T1 =

OFF time of Q1, T2 =

Time period, T = T1 + T2 =

Frequency, f =

RESULT:

Thus the Astable multivibrator is designed and its performance is tested.

Exp.No:3.B)NON-SINUSOIDAL WAVEFORM GENERATORS AND CONVERTERS (MONOSTABLE)

DATE:

AIM:

To set up a transistor monostable multivibrator circuit and (i) Plot the collector and base waveforms (ii) Measure the period of the pulse generated.

APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS/ COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	CRO	30 MHz	1
2.	Function generator	0 to 1 MHz	1
3.	Regulated PowerSupply (Dual)	5V	1
COMPONENTS REQUIRED			
4.	Diode	IN4001	1
5.	Capacitor	0.01µF	3
6.	Resistor [Passive]	4.7 KΩ, 5.6 KΩ, 47KΩ, 56 KΩ, 150KΩ	2, 1, 1, 1, 1
7.	Transistor [Active]	BC 548	2
8.	Bread Board	-	1
9.	Multimeter	-	1
10.	Connecting Wires	as required	

PRINCIPLE:

Astable multivibrator is also called free running multivibrator and is used as a square wave oscillator. The transistors in the circuit do not have stable state. i.e. when V_{cc} is given, one transistor turns ON (goes to saturation region) and the other turns OFF (goes to cut off region). After sometime (determined by charging and discharging of the two capacitors in the circuit), the ON transistor is turns OFF and the OFF transistor turns ON. This cycle repeats as long as the supply is given. When the power supply is turned ON, one of the transistors is ON and the other is OFF due to transistor mismatch. When Q_1 is ON, Q_2 is OFF due to the cross coupling. Collector of Q_1 is at V_{sat} ($\approx$ 0) and collector of Q_2 is at V_{cc}. Now the previously charged capacitor (when Q_2 is ON) discharges through Q_1 and after discharging completely it starts charging towards $V_{cc.}$ But as one side of the capacitor reaches 0.7V, Q_2 turns ON and its collector voltage falls to approximately 0V ($V_{ce\ sat}$). This sudden change is coupled to the base of Q_1 via

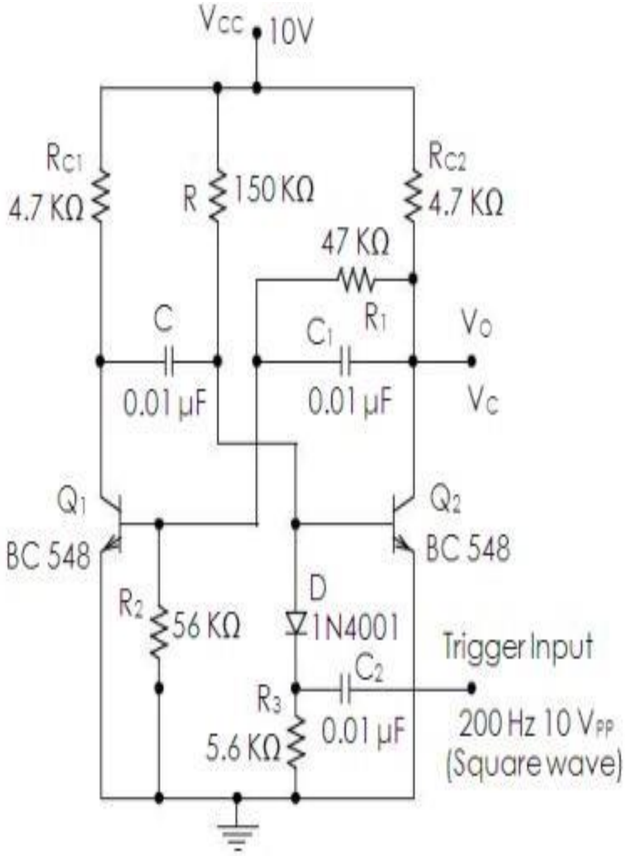
C_2. Thus Q_1 turns OFF and the collector of Q_1 reaches V_{cc}. Then C_2 (which was charged when Q_1 was ON), discharges through Q_2 and when other side of C_2 reaches 0.7V, Q_1 turns ON. These actions continue. Thus OFF time of Q_2 is determined by the values of R_1 and C_1 ($T_{OFFQ2} = 0.693\ R_1\ C_1$) while the OFF period of Q_1 is determined by the values of R_2 and C_2 ($T_{OFFQ1} = 0.693\ R_2\ C_2$). If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, we get a square wave from collector of the transistors. The time period of the square wave, $T = 0.693\ R_1\ C_1 + 0.693\ R_2\ C_2 = 1.38\ R\ C$ and $f = 1/T$.

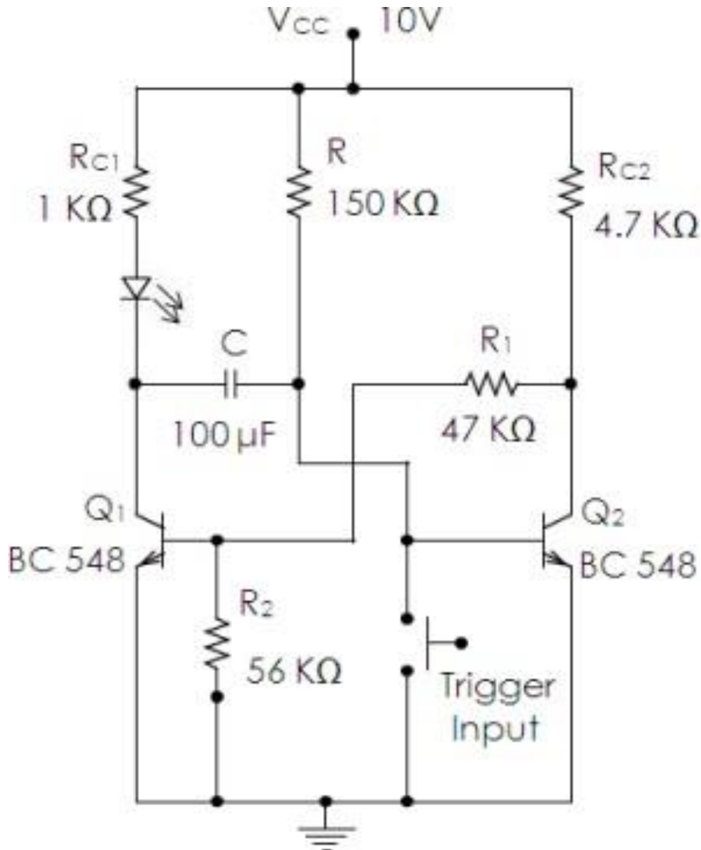
The second circuit is designed to get large ON and OFF periods for the transistors to visualize the ON and OFF action of transistors. For this LEDs are connected at the collector of the transistors. Here large value of C (10μF) is used to get T in seconds.

PROCEDURE:

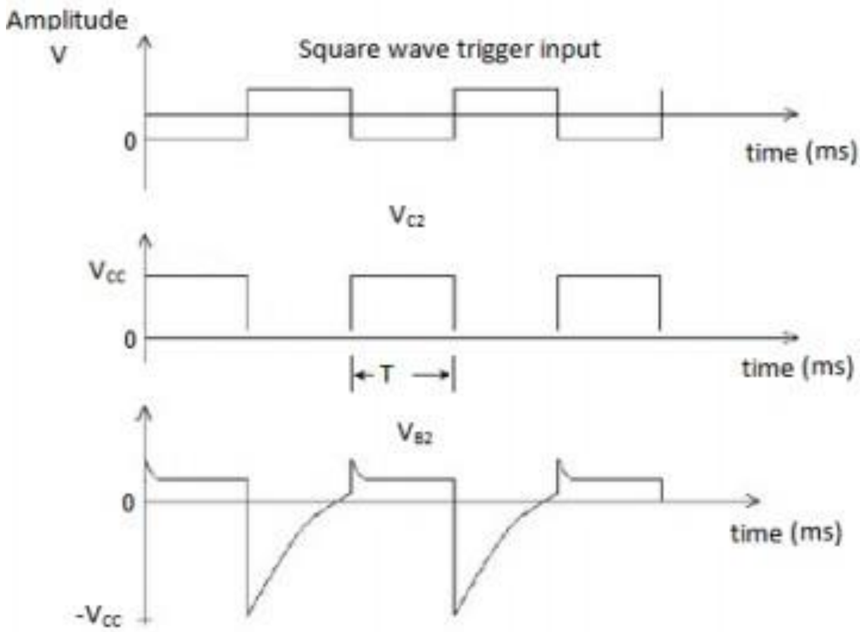
1. Test the components
2. Assemble the circuit in a breadboard
3. Switch ON the power supply
4. Connect the outputs of the circuit to an oscilloscope
5. Observe the collector and base waveforms of the two transistors
6. Measure the frequency and amplitude of the outputs
7. Plot all waveforms
8. Assemble the second circuit and visually verify the output

CIRCUIT DIAGRAM





MODEL GRAPH:



TABULATION:

TON =

TOFF =

Total T (TON + TOFF) =

RESULT:

Thus the Astable and Monostable multivibrators are designed and studied.

Exp.No:4.A) **DESIGN OF INTEGRATOR**

DATE:

AIM:

To design and construct RC integrator circuit and study its pulse response.

APPARATUS REQUIRED:

S.NO	NAME OF THEAPPARATUS/COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	CRO	30 MHz	1
2.	Function generator	0 to 1 MHz	1
COMPONENTS REQUIRED			
3.	Capacitor	22μF	1
4.	Resistor [Passive]	1KΩ	1
5.	Bread Board	-	1
6.	Multimeter	-	1
7.	Connecting Wires	as required	

PRINCIPLE:

An RC integrator circuit is a wave shaping circuit. It constitutes a resistor in series and a capacitor in parallel to the output. As the name suggests it does the mathematical operation „integration‟ on the input signal. The time constant RC of the circuit is very large in comparison with the time period of the input signal, under this condition the voltage drop across C will be very small in comparison with the voltage drop across R. For satisfactory integration it is necessary that RC ≥ 16T, where T is time period of the input.

When pulse waveform is given at the input, capacitor charges through R and output voltage builds up slowly. Capacitor continues to charge as long as input voltage is present. When input falls to zero, capacitor discharges and output falls to zero slowly. As the value of RC >> T, the charging current is almost constant and the output become linear. Hence a square pulse input provides a triangular output.

PROCEDURE:

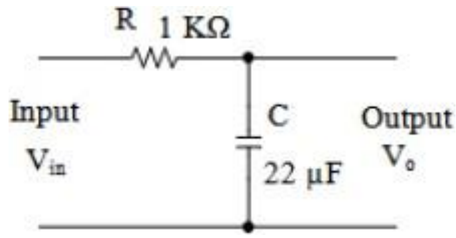
1. Test the components
2. Assemble the circuit on a breadboard
3. Connect the output of a function generator to the input of the integrator circuit
4. Switch on the function generator and set the input at 5V, 1KHz pulse

5. Connect the output of the integrator to an oscilloscope
6. Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input
    i. RC >> T (f = 1 KHz) that is RC >> 16T
    ii. RC > T (f = 100 Hz) o RC < T (f = 10 Hz) o RC << T (f = 1 Hz)
    iii. Study the behavior of the circuit for different values of T
7. Study the behavior of the circuit for different values of T
8. Plot all the input and output waveforms

RESULT:

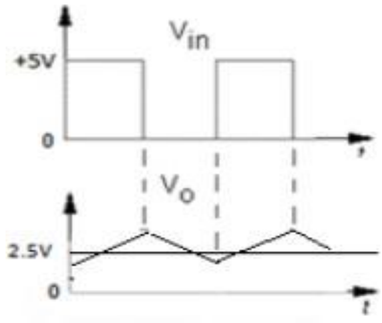
Thus the RC integrator circuit was designed and its pulse response was studied.

CIRCUIT DIAGRAM

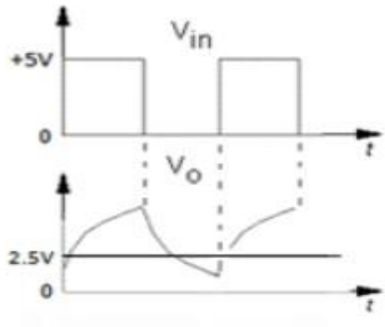


To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

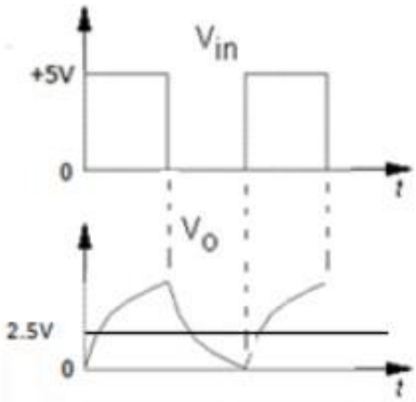
- f = 1 KHz, T =1/f = 1ms, RC = 22ms (RC >> T)



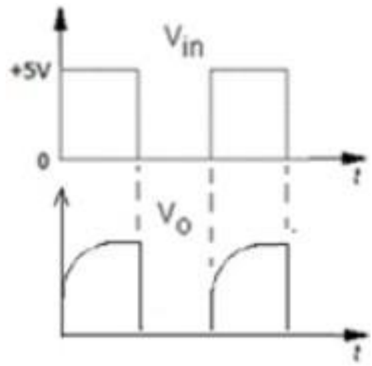
- f = 100 KHz, T =1/f = 10ms, RC = 22ms (RC > T)



- f = 10 Hz, T =1/f = 100ms, RC = 22ms (RC < T)



- f = 1 Hz, T =1/f = 1s, RC = 22ms (RC << T)



TABULATION:

Amplitude (Volts)	Time(ms)	Frequency (KHz)

Exp.No:4.B) **DESIGN OF DIFFERENTIATOR**

DATE:

AIM:

To design and construct RC differentiator circuit and study its pulse response.

APPARATUS REQUIRED:

S.NO	NAME OF THEAPPARATUS/COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	CRO	30 MHz	1
2.	Function generator	0 to 1 MHz	1
COMPONENTS REQUIRED			
3.	Capacitor	0.001μF	1
4.	Resistor [Passive]	1KΩ	1
5.	Bread Board	-	1
6.	Multimeter	-	1
7.	Connecting Wires	as required	

PRINCIPLE:

An RC differentiator circuit is a wave shaping circuit. It constitutes a capacitor in series and a resistor in parallel at the output. The time constant (R x C) of the circuit is very small in comparison with the period of the input signal. As the name shows the circuit does the mathematical operation „differentiation" on the input signal. At the time of differentiation the voltage drop across R will be very small in comparison with the drop across C.

Differentiated output is proportional to the rate of change of input. When the input rises to maximum value, differentiated outpour follows it, because the sudden change of voltage is transferred to the output by the capacitor. Since the rate of change of voltage is positive, differentiated output is also positive. When the input remains maximum for a period of time the rate of change of voltage is zero (of constant = Zero). During this time input acts like a dc voltage and capacitor blocks it (At this time the charge stored in the capacitor previously, discharges through R). When input falls to zero, rate of change is negative. Thus the output also goes to negative.

For perfect differentiation $RC < 0.0016T$ where $T = 1/f$ and f is the frequency of input signal.

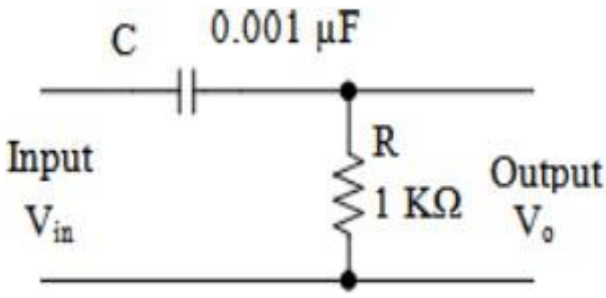
PROCEDURE:

1. Test the components
2. Assemble the circuit on a breadboard
3. Connect the output of a function generator to the input of the differentiator circuit
4. Switch on the function generator and set the input at 5V, 1KHz pulse
5. Connect the output of the differentiator to an oscilloscope.
6. Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input
    a. RC << T (f = 1 KHz) that is RC << 0.0016T
    b. RC < T (f = 100 KHz)
    c. RC > T (f = 1 MHz)
7. Study the behaviour of the circuit for different values of T
8. Plot all the input and output waveforms

RESULT:

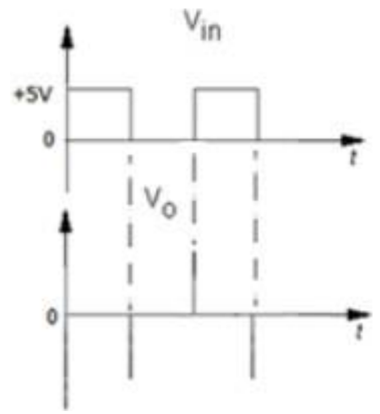
Thus the RC differentiator circuit was designed and its pulse response was studied.

CIRCUIT DIAGRAM:

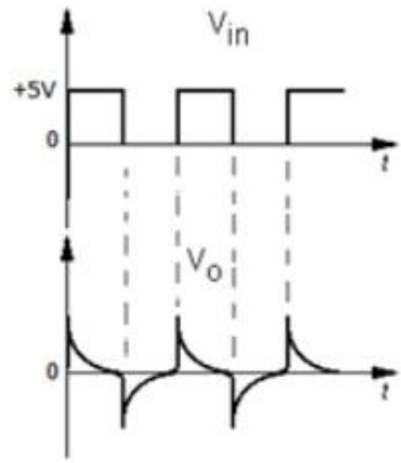


To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

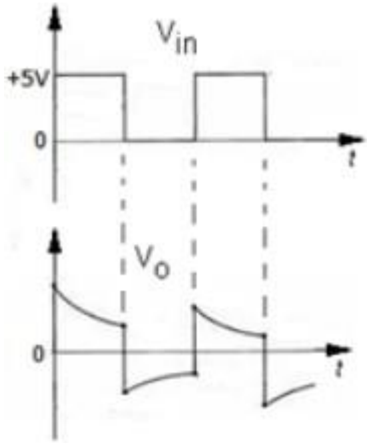
- f = 1 KHz, T = 1/f = 1ms, RC = 1µs (RC << T)



- f = 100 KHz, T = 1/f = 0.01ms, RC = 1µs (RC < T)



- f = 1 MHz, T = 1/f = 1μs, RC = 1μs (RC ≥ T)



TABULATION:

Amplitude (Volts)	Time(ms)	Frequency (KHz)

Exp.No:5. ANALYSIS OF FET, MOSFET WITH FIXED BIAS, SELF-BIAS AND VOLTAGE DIVIDER BIAS USING SIMULATION SOFTWARE

DATE:

AIM:

To simulate a FET, MOSFET with Fixed Bias, Self-Bias and Voltage Divider Bias using Simulation Software and to obtain its performance analysis.

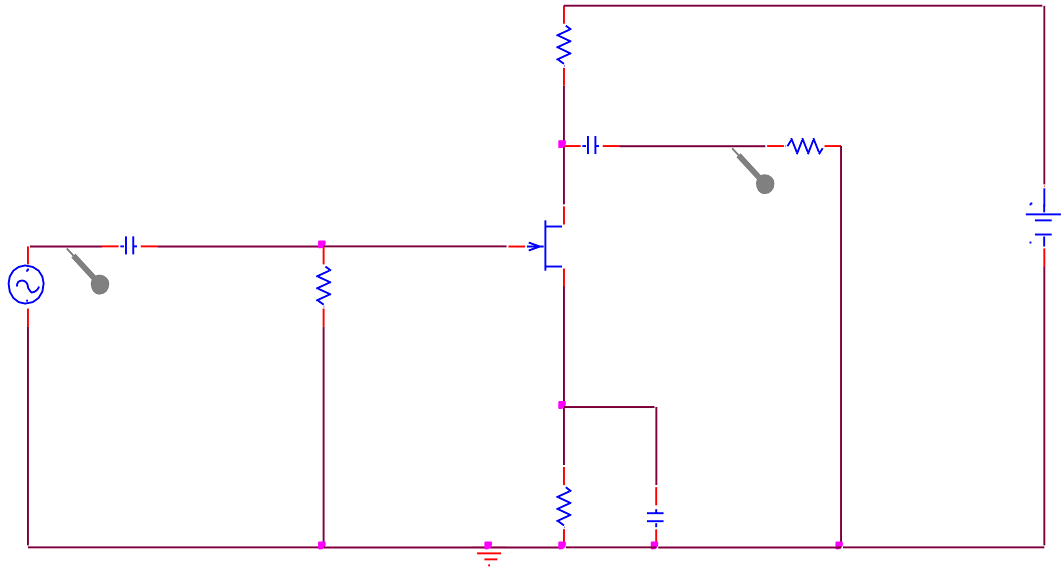
SOFTWARE REQUIRED:

ORCAD PSPICE

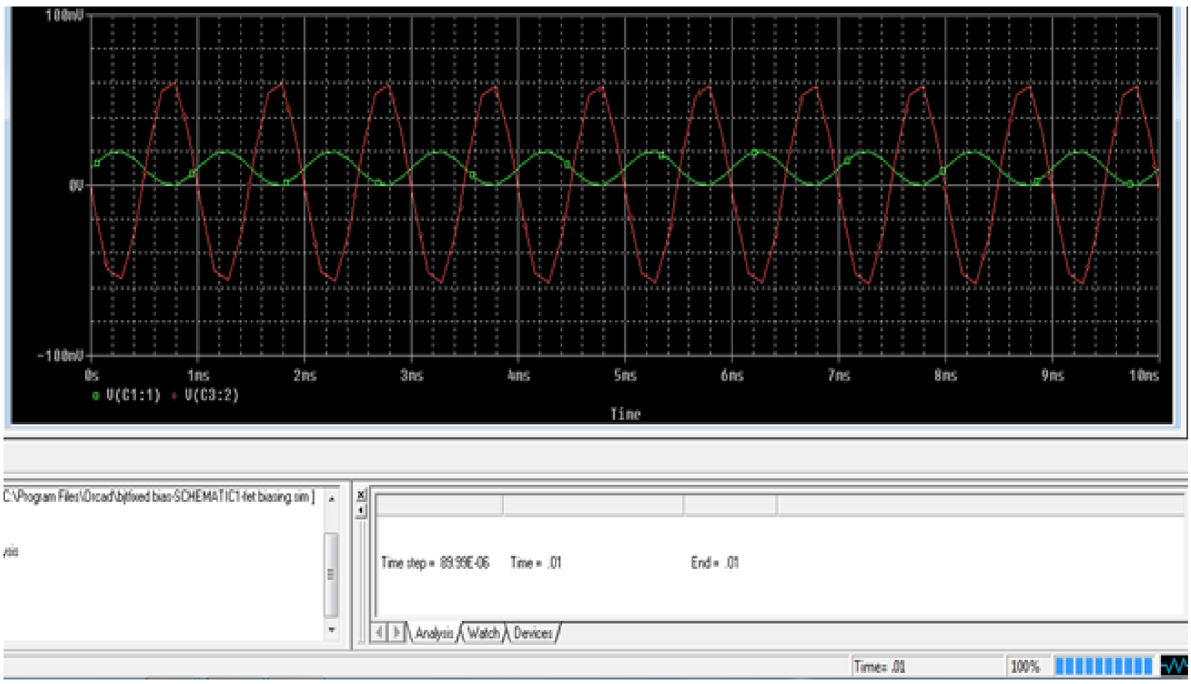
PROCEDURE:

1. Select File >> New >> Project. Name your project and select the directory as the location field. Be sure that you selected “Analog or Mixed A/D”.
2. Now, select “Create a blank project” at the appeared diagram box below.
3. An empty page in Schematic Editor will be opened. Now draw the given circuit in the Schematic Editor. To work your circuit properly, don’t forget to add Ground to your circuit. Set the parameters as shown in the circuit.
4. After the construction of the circuit, create a new profile using Pspice>> New Simulation Profile from toolbar. Write a name in the New Simulation Name.
5. After clicking on the Create button, the following dialog box will appear. For frequency response characteristics specify the type of analysis as “AC Sweep /Noise”. Since the input frequency is varied, enter the start frequency as 20Hz and end frequency as 20KHz. Enter the total number of points per decade in the Points/Decade box.
6. Run your program by using toolbar as Pspice>> Run.
7. Another window will be opened and the frequency response characteristics will be displayed.

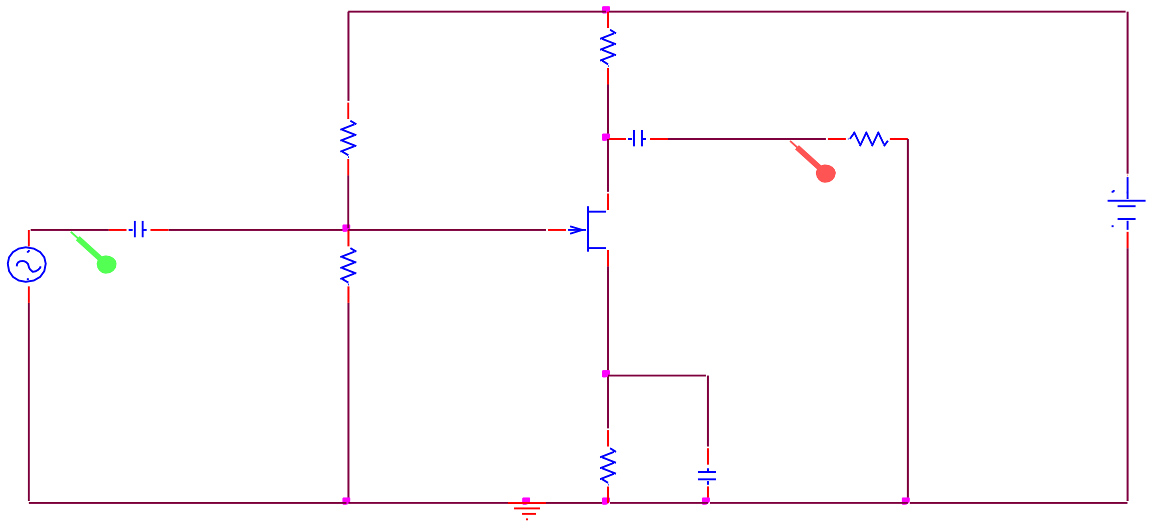
SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF FET WITH FIXED BIAS:



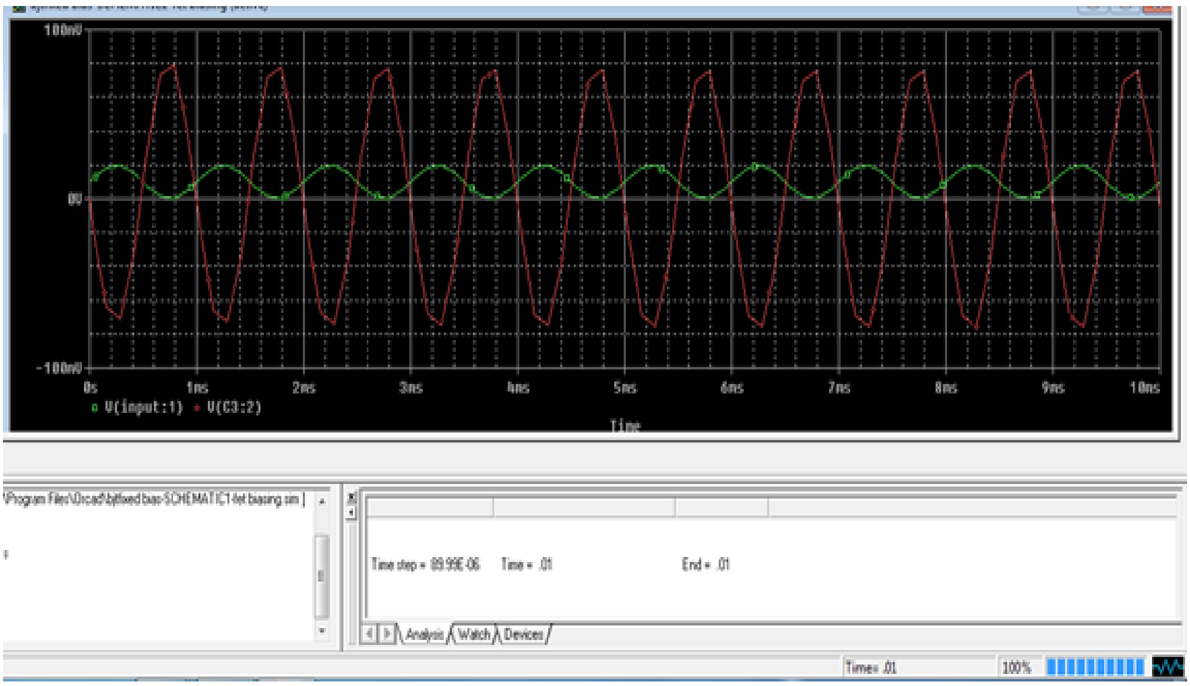
OUTPUT:



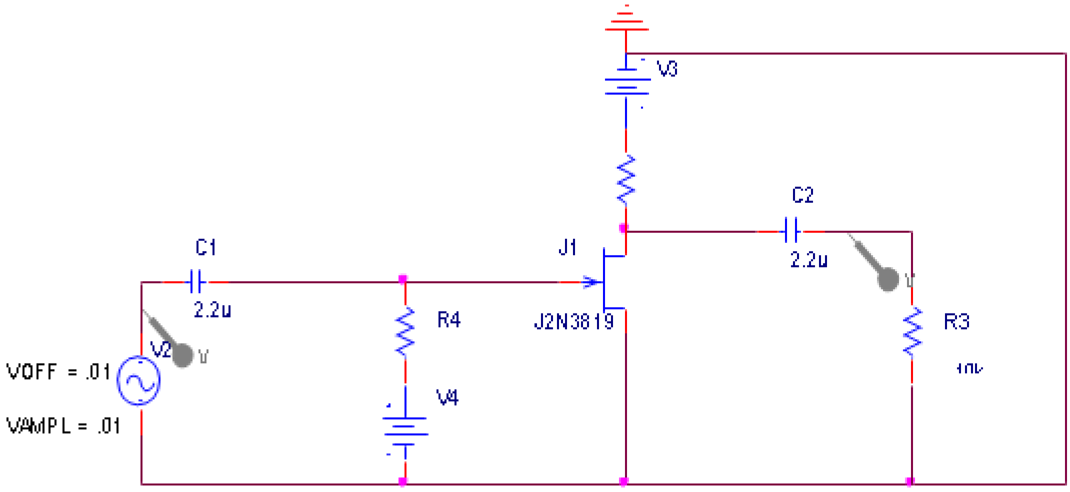
SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF FET WITH VOLTAGE DIVIDER BIAS:



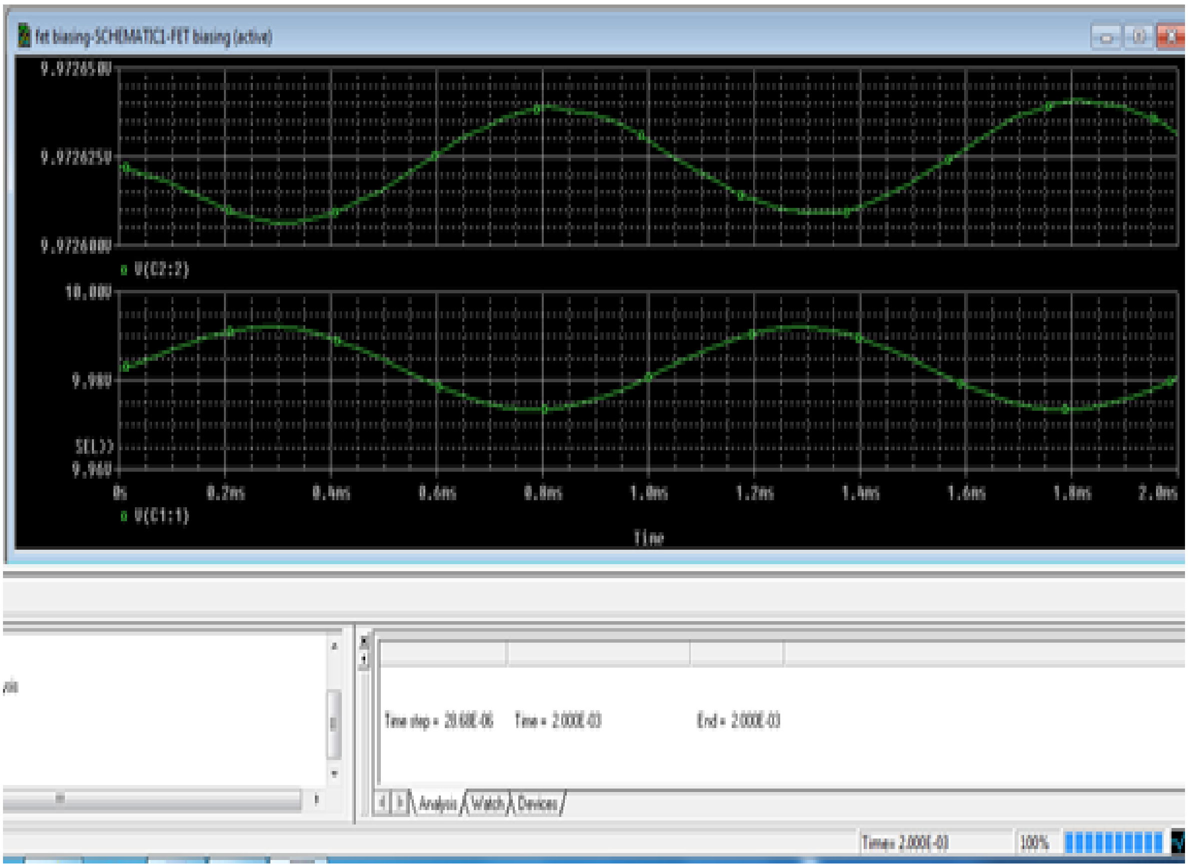
OUTPUT:



SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF FET SELF-BIAS:



OUTPUT:



Exp.No:6. DESIGN OF RC PHASE SHIFT OSCILLATOR, COLPITT AND WIEN BRIDGE OSCILLATOR USING SIMULATION SOFTWARE

DATE:

AIM:

To simulate a RC Phase Shift Oscillator, Colpitt Oscillator and Wien Bridge Oscillator using Simulation Software and to obtain its performance analysis.

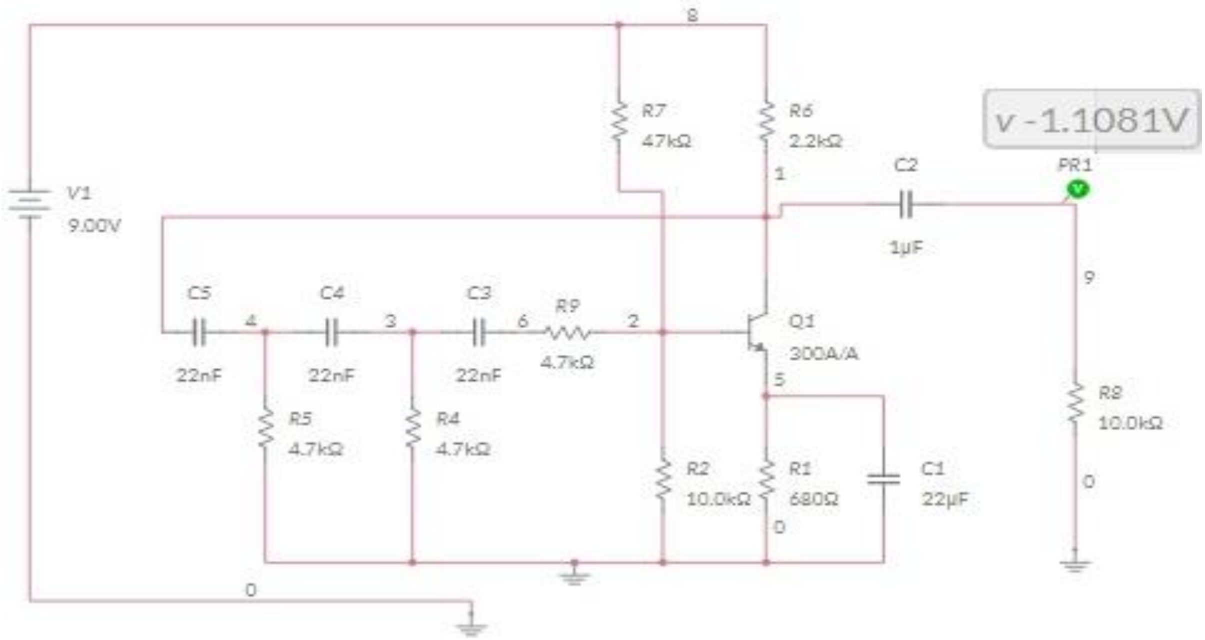
SOFTWARE REQUIRED:

ORCAD PSPICE

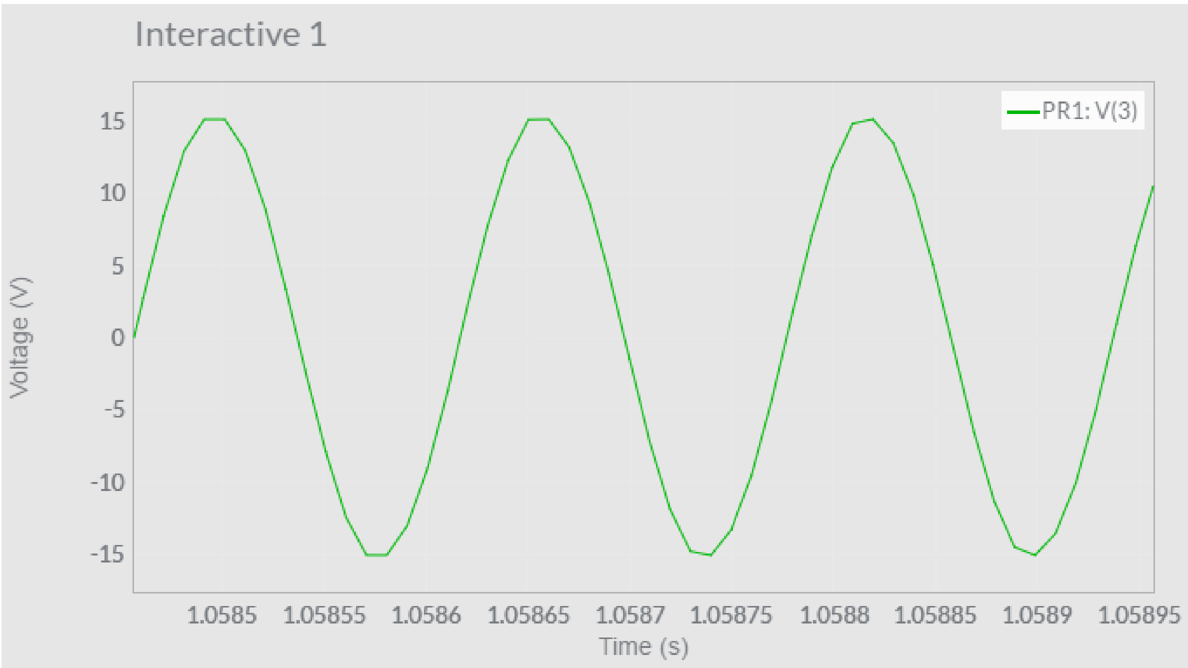
PROCEDURE:

1. Select File >> New >> Project. Name your project and select the directory as the location field. Be sure that you selected "Analog or Mixed A/D".
2. Now, select "Create a blank project" at the appeared diagram box below.
3. An empty page in Schematic Editor will be opened. Now draw the given circuit in the Schematic Editor. To work your circuit properly, don't forget to add Ground to your circuit. Set the parameters as shown in the circuit.
4. After the construction of the circuit, create a new profile using Pspice>> New Simulation Profile from toolbar. Write a name in the New Simulation Name.
5. After clicking on the Create button, the following dialog box will appear. For frequency response characteristics specify the type of analysis as "AC Sweep /Noise". Since the input frequency is varied, enter the start frequency as 20Hz and end frequency as 20KHz. Enter the total number of points per decade in the Points/Decade box.
6. Run your program by using toolbar as Pspice>> Run.
7. Another window will be opened and the frequency response characteristics will be displayed.

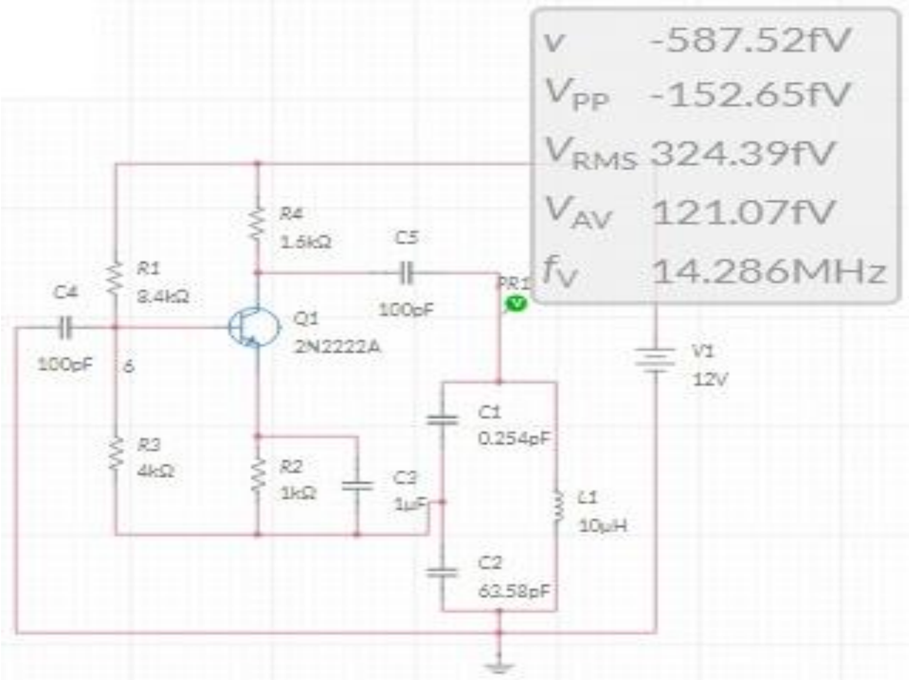
SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF RC PHASE SHIFT OSCILLATOR:



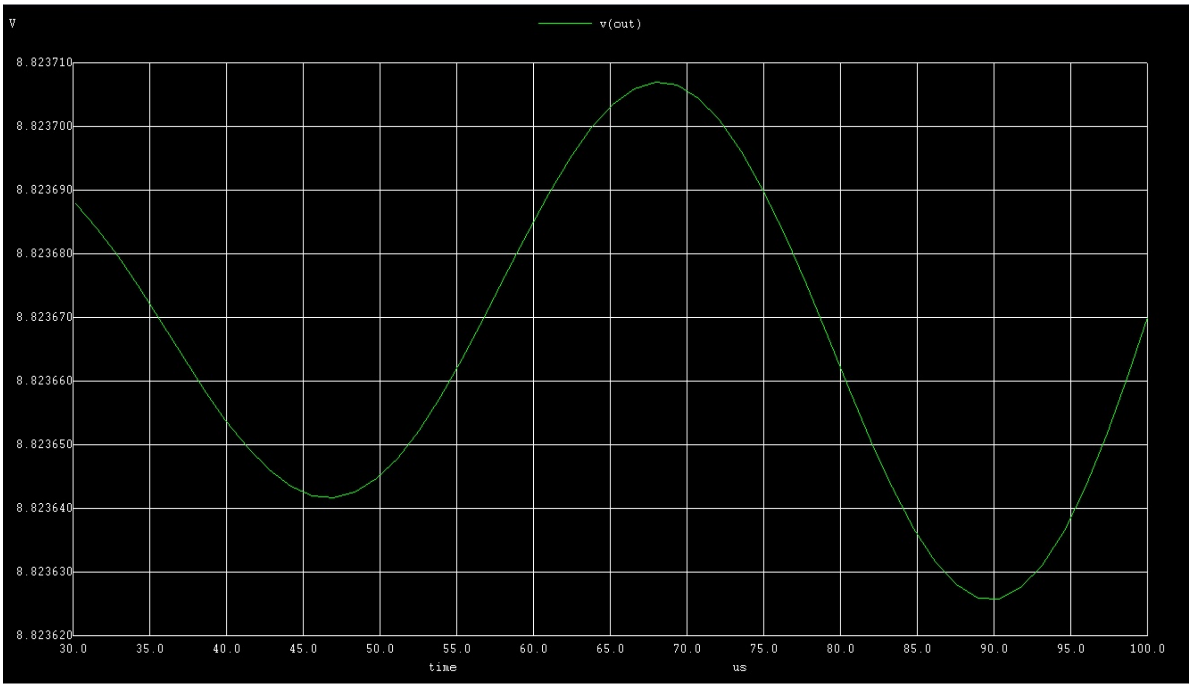
OUTPUT:



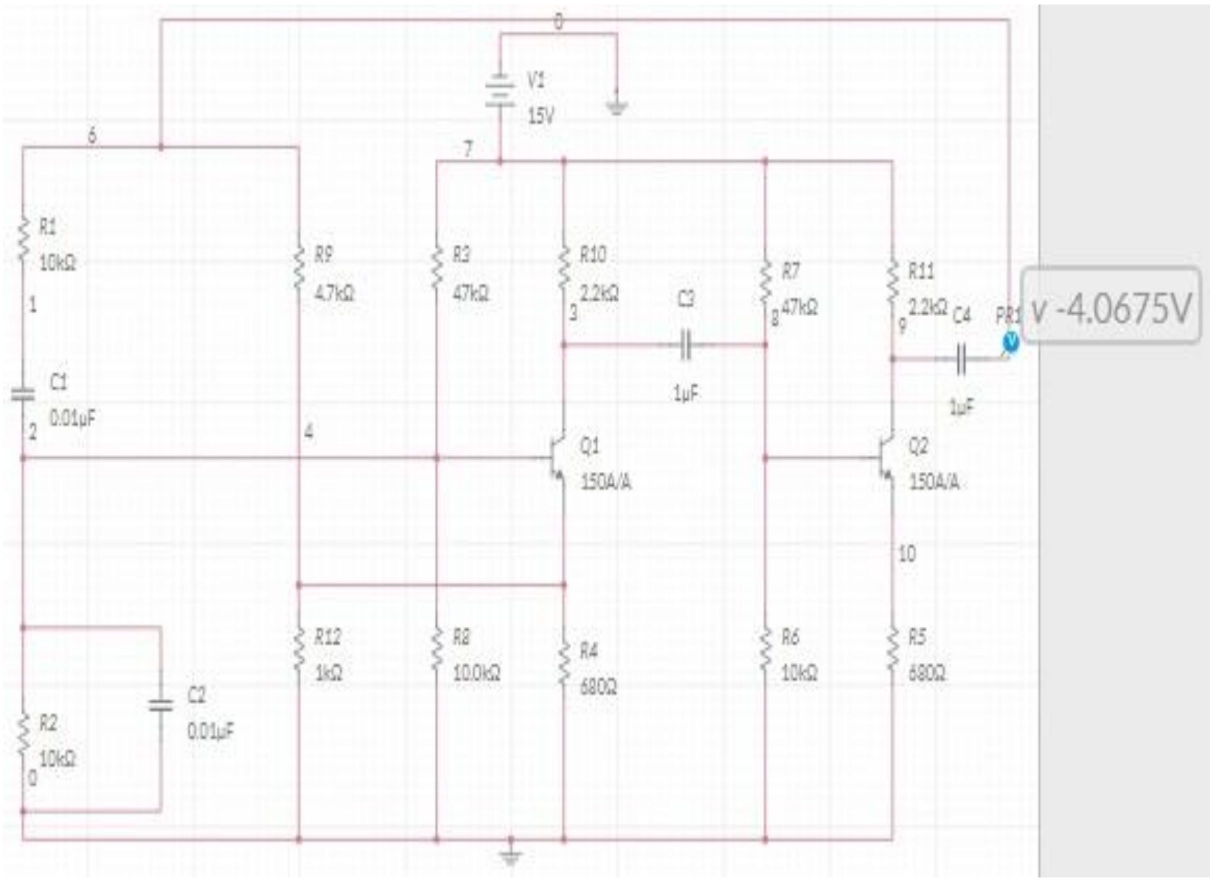
SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF COLPITT OSCILLATOR:



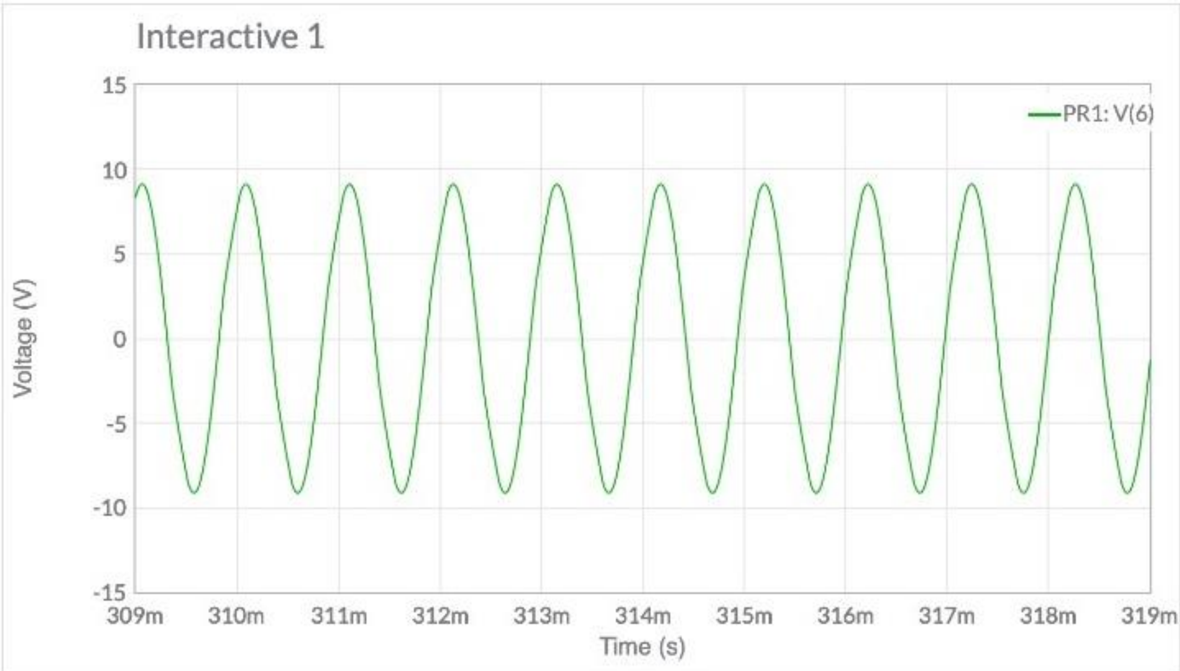
OUTPUT:



SCHEMATIC DIAGRAM AND PERFORMANCE ANALYSIS OF WIEN BRIDGE OSCILLATOR:



OUTPUT:



RESULT:

Thus BJT with RC Phase Shift, Colpitt and Wien Bridge Oscillators ORCAD PSPICE is simulated and their performance analysis is obtained.

Exp.No:--- **STUDY OF LOGIC GATES**

DATE:

AIM:

To Study and verify the truth table of various basic Logic Gates.

APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS / COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Digital IC Trainer Kit	-	1
COMPONENTS REQUIRED			
2.	NAND GATE	IC 7400	1
3.	NOR GATE	IC 7402	1
4.	NOT GATE	IC 7404	1
5.	AND GATE	IC 7408	1
6.	OR GATE	IC 7432	1
7.	EX-OR GATE	IC 7486	1
8.	Connecting Wires	as required	

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE:

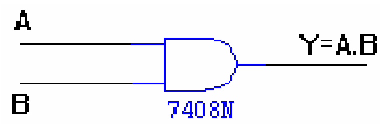
The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

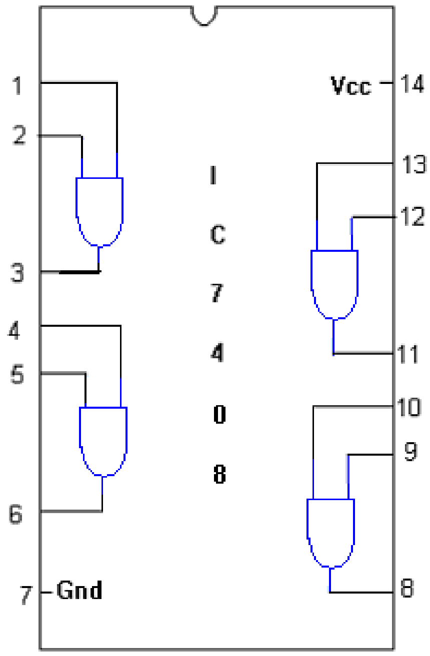
PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

AND GATE:

SYMBOL:



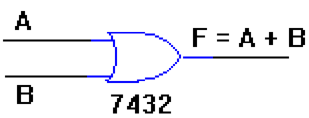


TRUTH TABLE

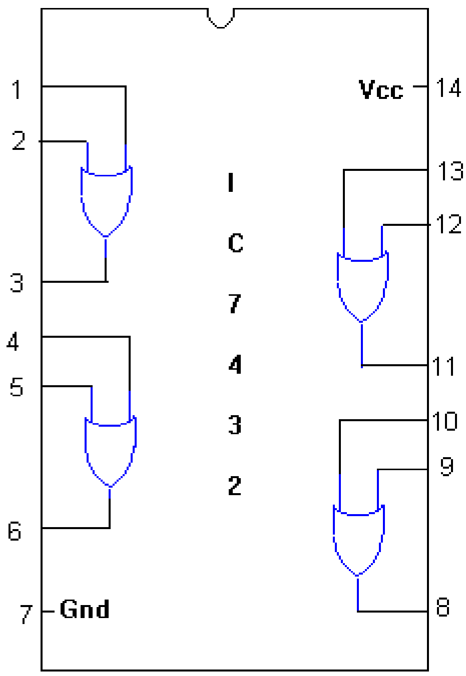
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

SYMBOL:



PIN DIAGRAM :

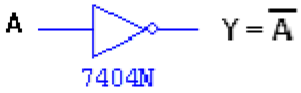


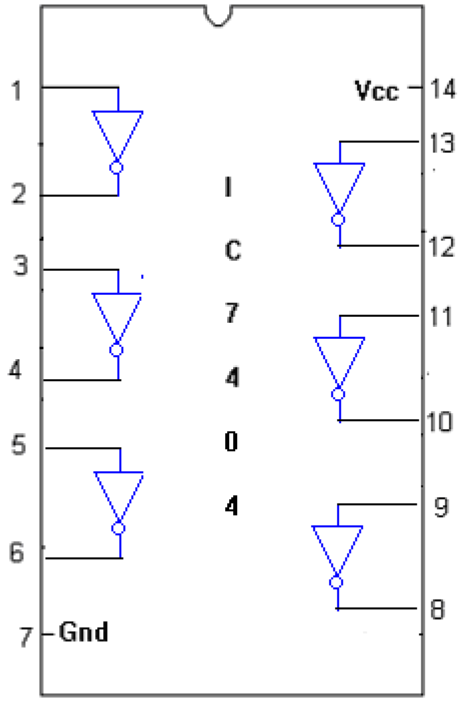
TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

SYMBOL:



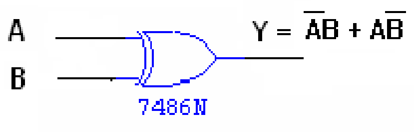


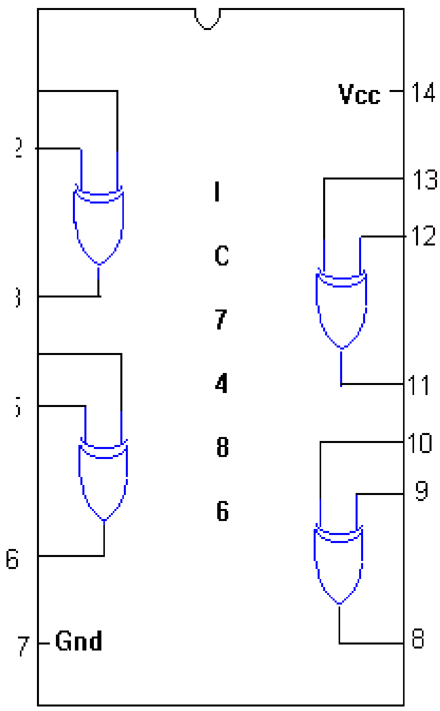
TRUTH TABLE :

A	$\overline{A}$
0	1
1	0

XOR GATE:

SYMBOL:



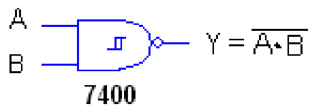


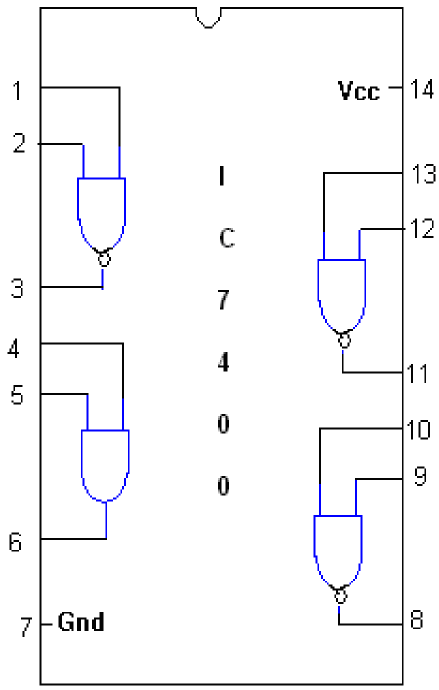
TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

NAND GATE:

SYMBOL: (2 INPUT)





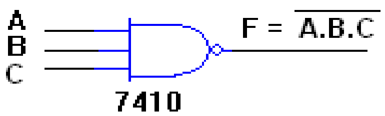
TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

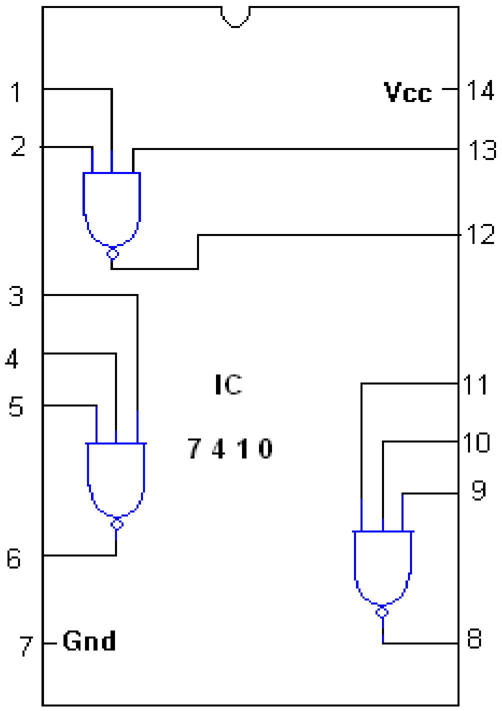
NAND GATE:

SYMBOL: (3 INPUT)

SYMBOL :



PIN DIAGRAM :

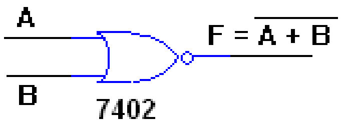


TRUTH TABLE

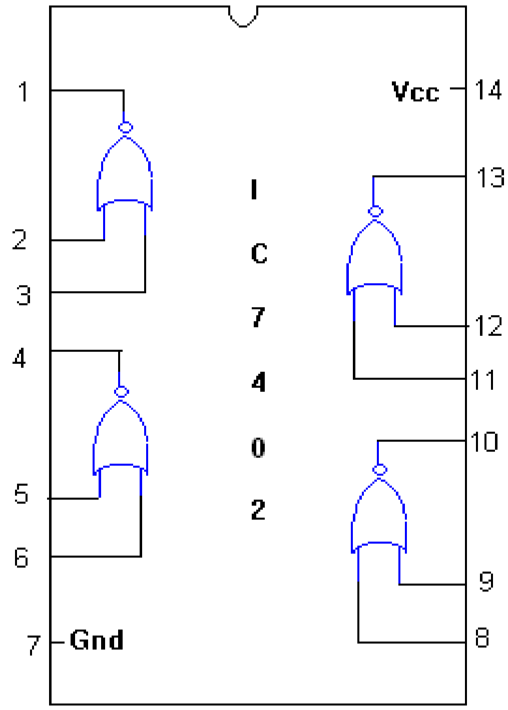
A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

NOR GATE:

SYMBOL:



PIN DIAGRAM :



TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

RESULT:

Thus the various Logic gate truth tables were verified.

Exp.No:7 DESIGN OF HALF ADDER AND FULL ADDER USING BASIC GATES

DATE:

AIM:

To design and construct a half adder and full adder circuit and also verify the truth table using logic gates.

APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS / COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Digital IC Trainer Kit	-	1
COMPONENTS REQUIRED			
2.	OR GATE	IC 7432	1
3.	EX-OR GATE	IC 7486	1
4.	AND GATE	IC 7408	1
5.	Connecting Wires	as required	

THEORY:

HALF ADDER:

A half adder has two inputs for the two bits to be added and two outputs one from the sum ' S' and other from the carry ' c' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

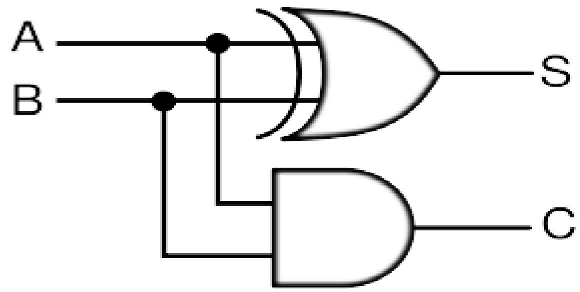
FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

PROCEEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

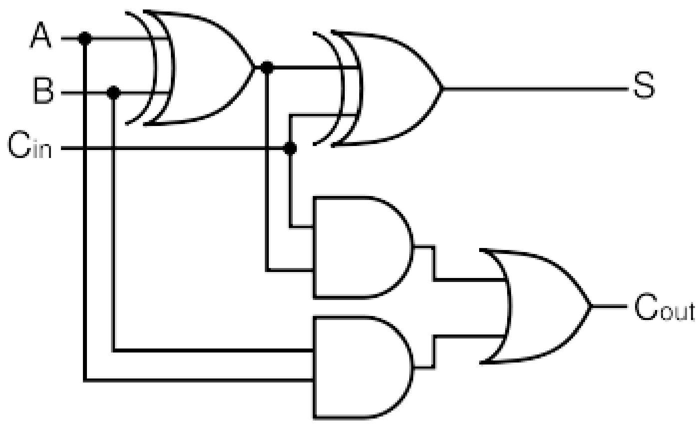
HALF ADDER LOGIC DIAGRAM:



HALF ADDER - TRUTH TABLE:

INPUT		OUTPUT	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER LOGIC DIAGRAM:



FULL ADDER - TRUTH TABLE:

INPUT			OUTPUT	
A	**B**	**Cin**	**SUM**	**CARRY**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

RESULT:

Thus the half adder and full adder circuit using logic gates was designed and implemented successfully.

Exp.No:8 DESIGN OF MULTIPLEXER AND DEMULTIPLEXER USING BASIC GATES

DATE:

AIM:

To design and construct a multiplexer and de- multiplexer circuit and also to verify the truth table using logic gates.

APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS / COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Digital IC Trainer Kit	-	1
COMPONENTS REQUIRED			
2.	NOT GATE	IC 7404	1
3.	AND GATE	IC 7411	2
4.	OR GATE	IC 7432	1
5.	Connecting Wires	as required	

THEORY:

MULTIPLEXER:

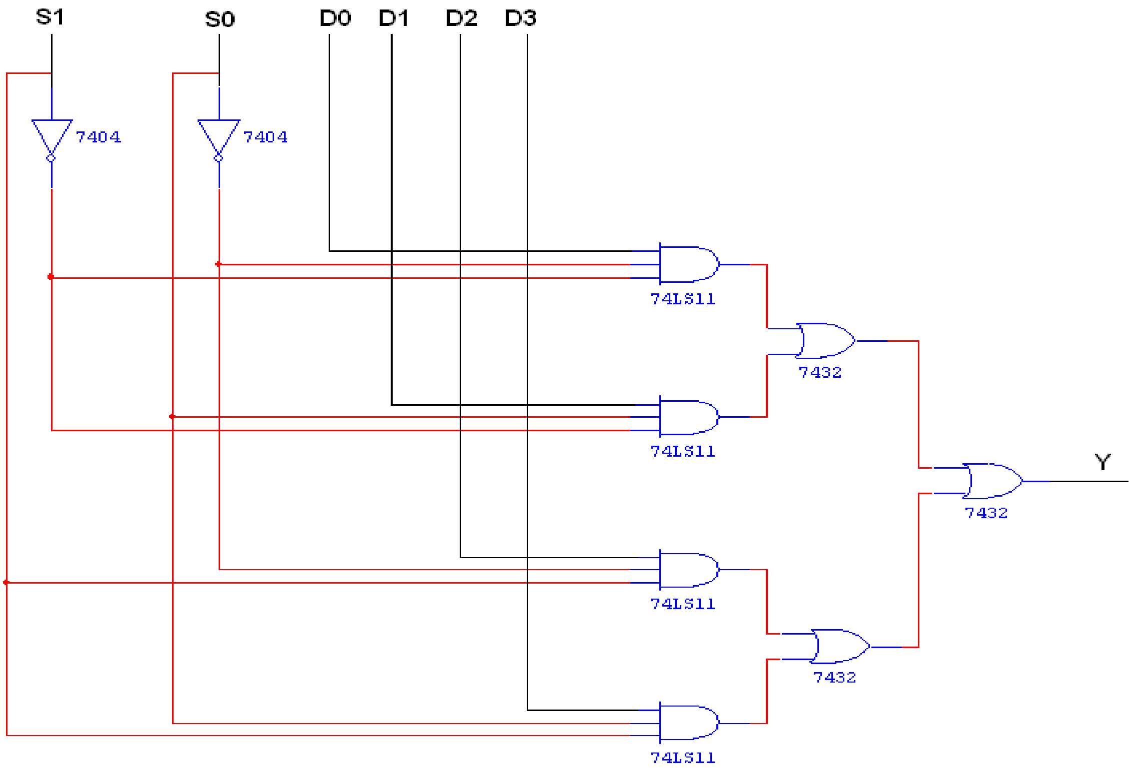
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

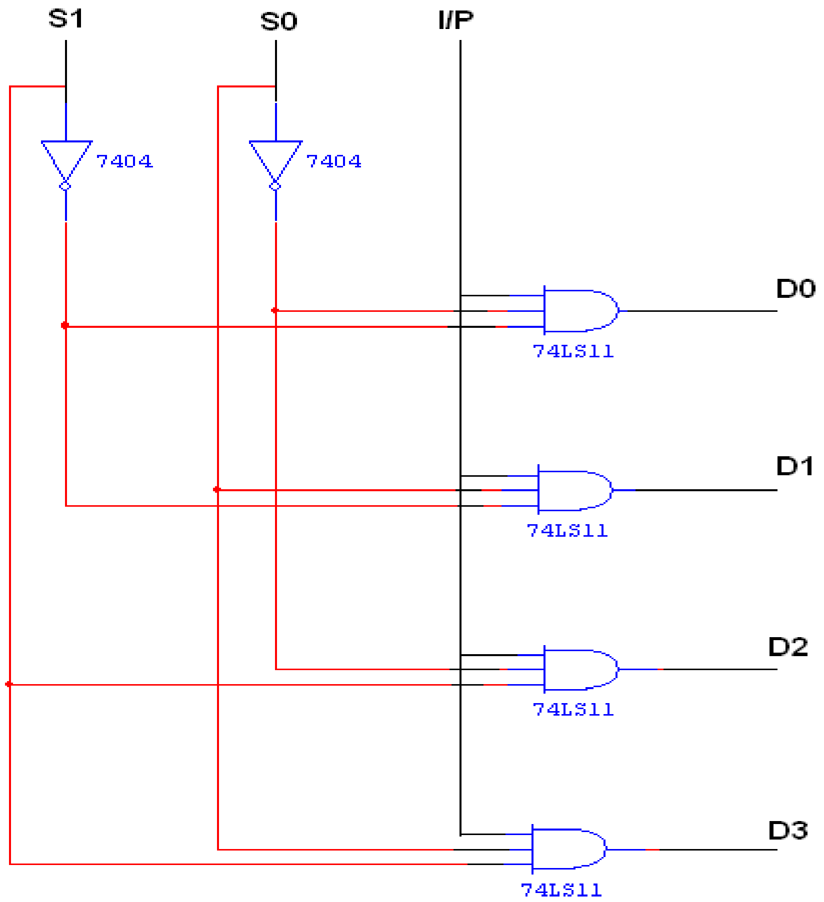
LOGIC DIAGRAM FOR MULTIPLEXER (4:1 MUX):



TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

LOGIC DIAGRAM FOR DE-MULTIPLEXER (1:4 DE-MUX):



TRUTH TABLE:

INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

PROCEEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

RESULT:

Thus a multiplexer and de-multiplexer using logic gates was designed and implemented successfully.

Exp.No:9 **DESIGN OF CODE CONVERTERS USING LOGIC GATES**

(BINARY TO GRAY AND VICE – VERSA)

DATE:

AIM:

To design and construct a Binary to Gray code converter and Gray to Binary code converter circuits and also to verify the truth table using logic gates.

APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS / COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Digital IC Trainer Kit	-	1
COMPONENTS REQUIRED			
2.	XOR GATE	IC 7486	1
3.	Connecting Wires	as required	

THEORY:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

The input variable are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, Co. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a function of the four input variables.

A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit. Now the OR gate whose output is C+D has been used to implement partially each of three outputs.

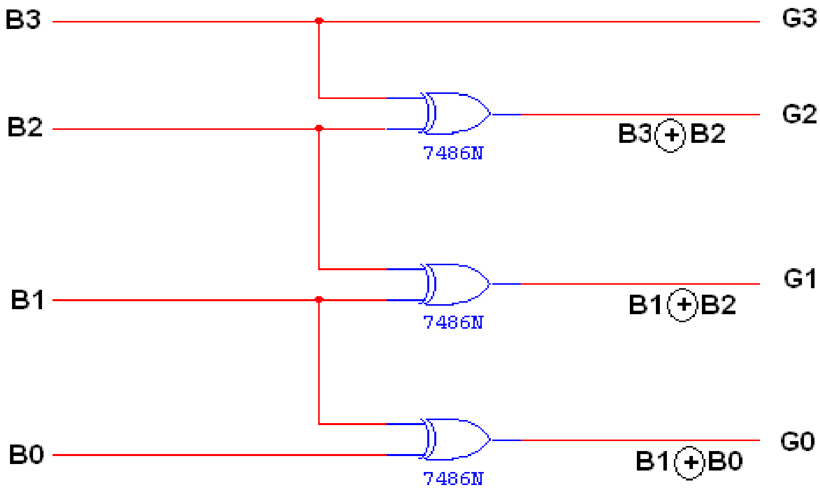
PROCEEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

RESULT:

Thus a multiplexer and de-multiplexer using logic gates was designed and implemented successfully.

LOGIC DIAGRAM FOR BINARY TO GRAY CODE CONVERTER:



K-Map for G_3:

B3B2 \ B1B0	00	01	11	10
00				
01				
11	1	1	1	1
10	1	1	1	1

$G_3 = B_3$

K-Map for G_2:

B3B2 \ B1B0	00	01	11	10
00				
01	1	1	1	1
11				
10	1	1	1	1

$G_2 = B_3 \text{ XOR } B_2$

K-Map for G_1:

B3B2 \ B1B0	00	01	11	10
00			1	1
01	1	1		
11	1	1		
10			1	1

$G_1 = B_2 \text{ XOR } B_1$

K-Map for G_0:

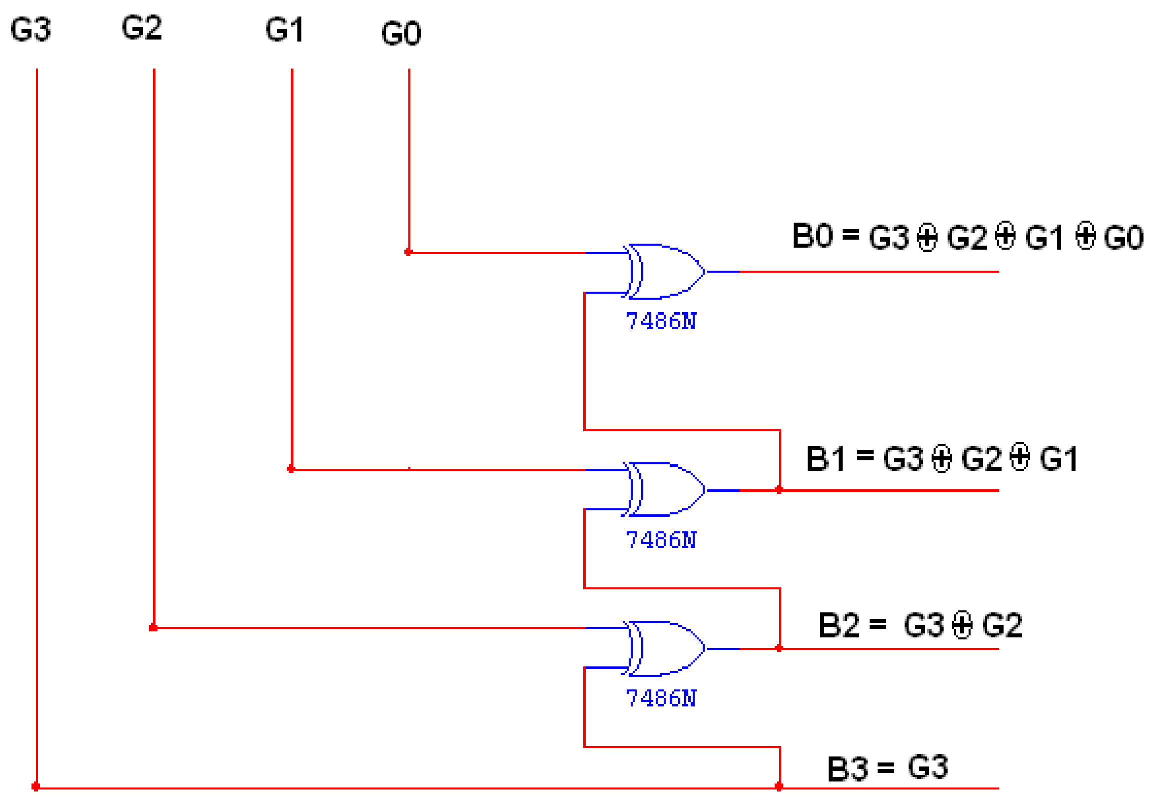
B3B2 \ B1B0	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

$G_0 = B_1 \text{ XOR } B_0$

TRUTH TABLE:

BINARY INPUT				GRAY OUTPUT			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

LOGIC DIAGRAM FOR GRAY CODE TO BINARY CONVERTER:



K-Map for B_3:

G3G2 \ G1G0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$B_3 = G_3$

K-Map for B_2:

G3G2 \ G1G0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$B_2 = G_3$ XOR G_2

K-Map for B_1:

G3G2 \ G1G0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	0	0	1	1
10	1	1	0	0

$B_1 = G_3$ XOR G_2 XOR G_1

K-Map for B_0:

G3G2 \ G1G0	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$B_1 = G_3$ XOR G_2 XOR G_1 XOR G_0

TRUTH TABLE:

GRAY INPUT				BINARY OUTPUT			
G_3	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Exp.No:10 **DESIGN OF SYNCHRONOUS RIPPLE COUNTERS**

DATE:

AIM:

To design and verify the synchronous ripple counters.

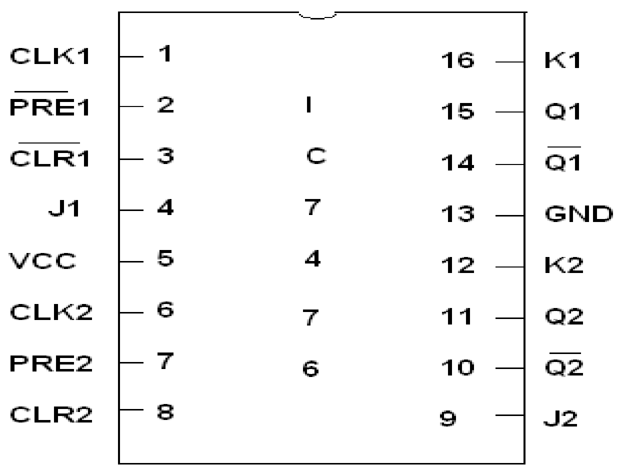
APPARATUS REQUIRED:

S.NO	NAME OF THE APPARATUS / COMPONENTS	RANGE	QUANTITY
APPARATUS REQUIRED			
1.	Digital IC Trainer Kit	-	1
COMPONENTS REQUIRED			
2.	JK FLIP FLOP	IC 7476	2
3.	Connecting Wires	as required	

THEORY:

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous counter a common clock is given to all flip flops and in asynchronous counter the first flip flop is clocked by external pulse and then each successive flip flop is clocked by the Q output of the previous stage. The clock of the second stage is triggered by the output of the first stage. Because of inherent propagation delay time, all flip flops are not activated at same time which results in asynchronous operation.

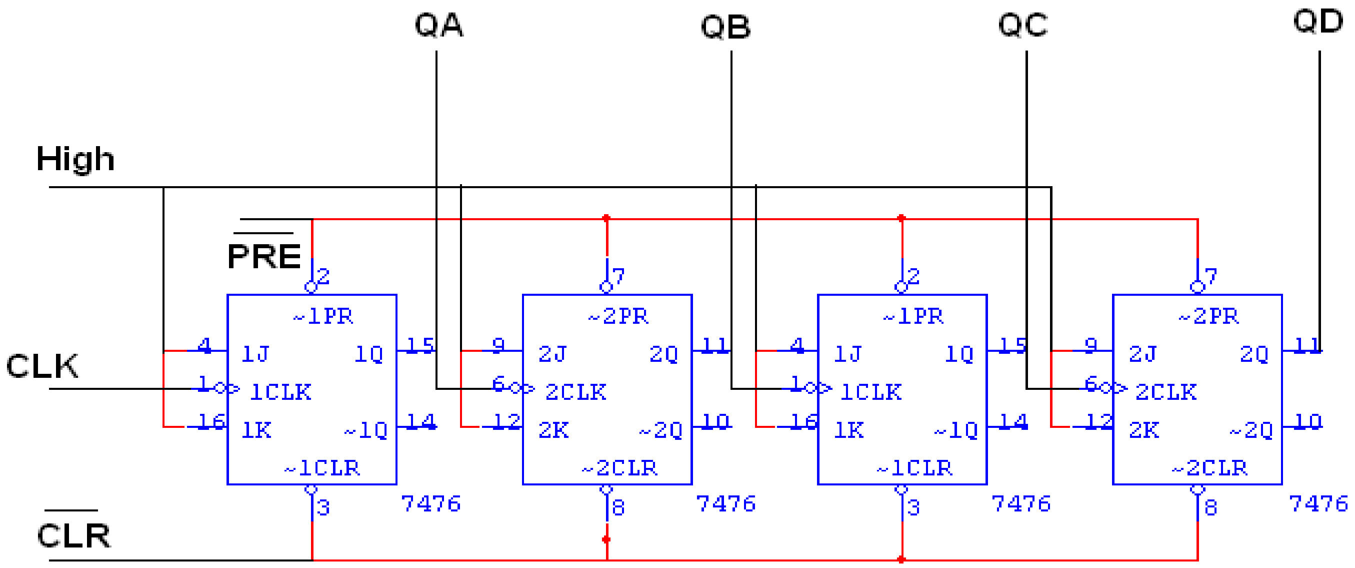
PIN DIAGRAM OF IC 7476:



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

LOGIC DIAGRAM FOR 4 BIT RIPPLE COUNTER:



PROCEEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

RESULT:

Thus a 4 Bit ripple counter was constructed and verified successfully.