Integrated circuits and operational Amplifier

Definition of IC : The Integrated circuit (or) IC is a miniature, low cost electronic circuit consisting of active and passive components that are inseparably joined together on a single crystal chip of silicon.

Advantages of IC's :

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance
5. Increased operating speeds
6. Reduction in power consumption.

Classification of IC's :

I **Based on mode of operation :**

a) Digital IC's b) Linear IC's

a) **Digital IC's :** Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.

Ex : Gates, counters, multiplexers, demultiplexers, shift registers.

Linear Ic's: Linear Ic's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers and modulators that often require additional external components for satisfactory operation.

Ex: op-Amps

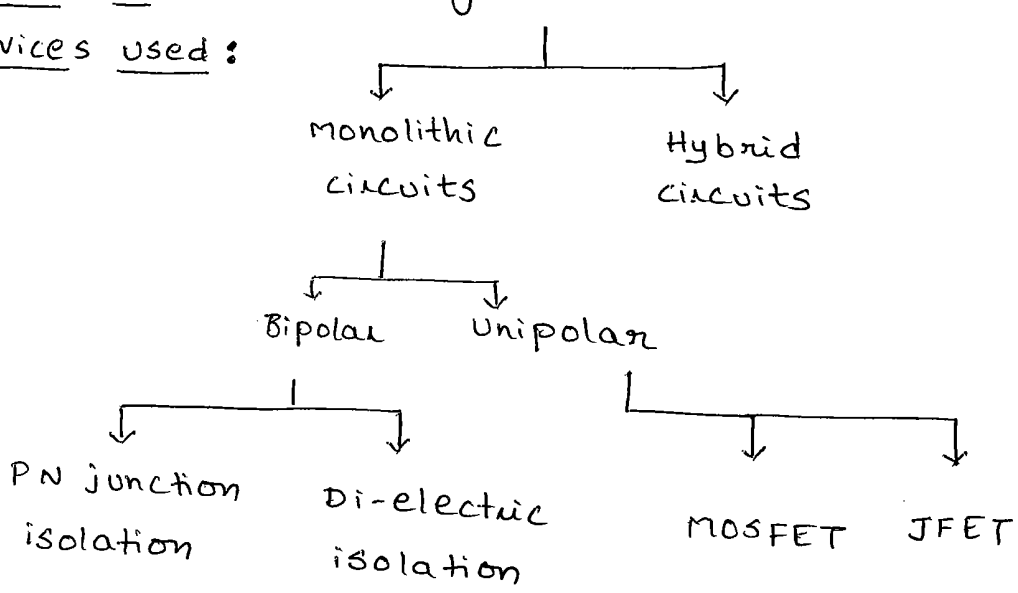
II Based on Fabrication

a) Monolithic Ic's b) Hybrid Ic's

a) Monolithic Ic's: In monolithic Ic's all components (active and passive) are formed simultaneously by a diffusion process. then a metallization process is used in interconnecting these components to form the desired circuit.

b) Hybrid Ic's: In Hybrid Ic's, passive components (such as resistors and capacitors) and the interconnections between them are formed on an insulating substrate. The substrate is used as a chassis for the integrated components. Active components such as transistors and diodes as well as monolithic integrated circuits, are then connected to form a complete circuit.

(iii) Based on devices used:



IC chip size and circuit complexity:

The concept of IC was introduced at the begining of 1960 by both Texas instruments and Fairchild Semi Conductors. Since that time, the size and complexity of IC's have increased rapidly as shown by the brief chronology.

1. Invention of Transistor		1947
2. Development of Si Transistor		1955 - 1959
3. Si planar Technology	junction transistor diode	1959
4. First IC, small scale integration	3 to 30 gates/chip approx. (or) 100 transistors / chip (Logic Gates, Flipflops)	1960 - 65

5. Medium scale Integration (MSI)	30 to 300 gates/chip (or) 100 to 1000 transistors per chip. (counters, Mux's, Adders)	1965 - 1970
6. Large Scale Integration (LSI)	300 to 3000 gates/chip (or) 1000 to 20000 transistors per chip (8 bit µP's, ROM, RAM)	1970 - 1980
7. Very large scale Integration (VLSI)	More than 3000 gates/chip (or) 20,000 - 1000000 transistors/Chip (16 and 32 bit µP's)	1980 - 1990
8. Ultra large scale integration (ULSI)	10^6 to 10^7 transistors/chip (special processors, virtual reality machines, smart sensors)	1990 - 2000
9. Giant - scale Integration	> 10^7 transistors/chip	

Manufacturers Designations for integrated circuits

Each manufacturer uses a specific code and assigns a specific type number to the IC's it produces. That is, each manufacturer uses its own identifying initials followed by its own type number.

For example, the 741 type of internally compensated op-Amp was originally manufactured by Fairchild and is sold as the μA741, where μA represents the identifying initials used by fairchild. Initials used by some of the well known manufacturers of linear IC's are as follows

Fairchild	: μA, μAF
National Semiconductor	: LM, LH, LF, TBA
Motorola	: MC, MFC
Texas instruments	: SN
RCA	: CA, CD
signetics	: N/S, NE/SE, SU
Burr Brown	: BB

Fairchild's original μA741 is also manufactured by various other manufacturers under their own designations, as follows.

National semiconductor	LM741
Motorola	MC1741
RCA	CA3741
Texas Instruments	SN 52741
Signetics	N5741.

Temperature ranges of Ic's :

All Ic's manufactured fall in to one of the three basic temperature grades.

1. Military temperature range $-55^{\circ}c$ to $125^{\circ}c$
2. Industrial temperature range $-20^{\circ}c$ to $+85^{\circ}c$
3. Commercial temperature range $0^{\circ}c$ to $+70^{\circ}c$.

Applications of IC

Ic's have become a vital part of modern electronic circuit design. They are used in

1. Computer Industry
2. Automobile Industry
3. Home appliances
4. Communication
5. Control systems

where they permit miniaturization and superior performance not possible with discrete components.

OPERATIONAL AMPLIFIER (OP-AMP)

* An Important Linear IC is operational Amplifier.
* The operational Amplifier is a multiterminal device which internally is quite complex.
* OP-Amp is a direct coupled high gain Amplifier
* OP-Amp can be used to amplify both a.c and d.c signals.
* It is used to perform a Variety of mathematical operations such as Addition, subtraction, log, Antilog, Differentiation, Integration etc. Hence the Due to its use in performing mathematical operations, it has been given a name 'operational Amplifier'
* Earlier op-Amps were designed by using Vaccum tubes, Hence the op-Amps were bulky, power consuming and expensive.
* Between 1964 to 1968 the popular 741 integrated circuit op-Amp was introduced by Robert.j.widlar
* The IC Version of op-Amp uses BJT's and FET's which are fabricated along with the other supporting components on a single semiconductor chip.

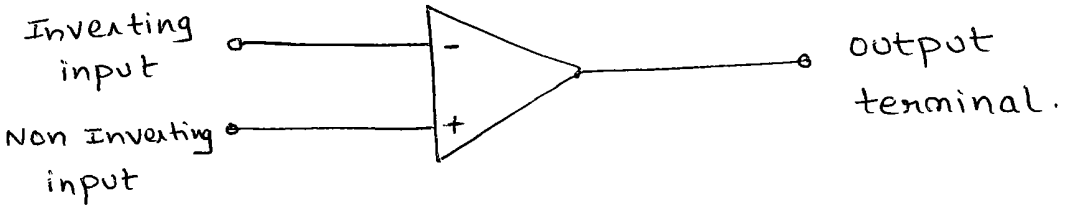
Advantages: Low cost, small size, Versatile, flexible

Applications :

communications, computers, power and signal sources, process control, displays and measuring systems.

Op-Amp Symbol and Terminals :

Op-Amp symbol : The circuit schematic of an Op-Amp is a triangle as shown in figure below. It has two input terminals and one output terminal



Packages :

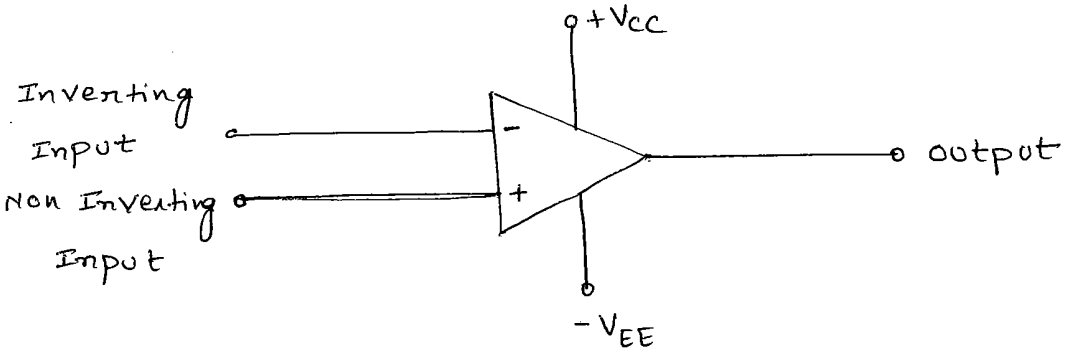
There are three popular packages available

1. The metal can (TO) package
2. The flat package (or) flat pack
3. the dual-in-line package (DIP)

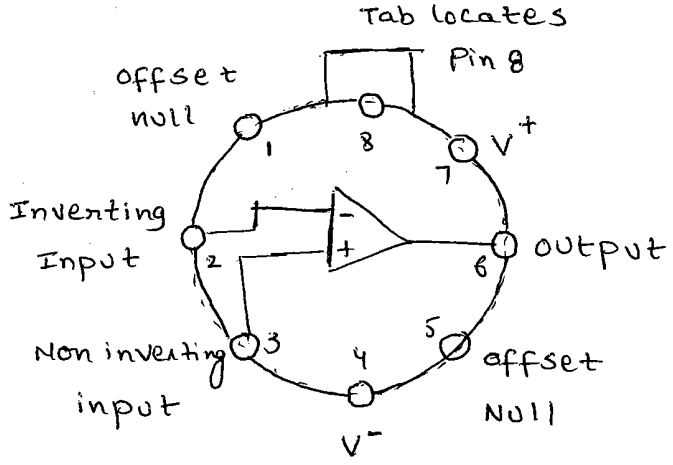
Op-Amp Terminals :

Op-Amps have five basic terminals, that is

1. Two input terminals
2. one output terminal
3. Two power supply terminals.

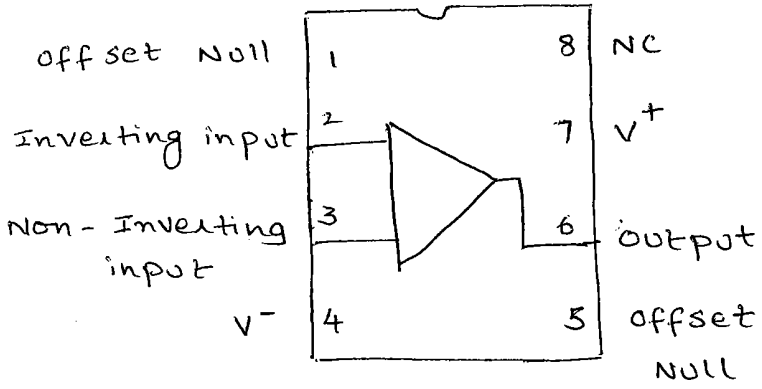


The IC 741 8-Pin Metal Can is shown in figure below.



Fig(a): 8 Pin Metal can

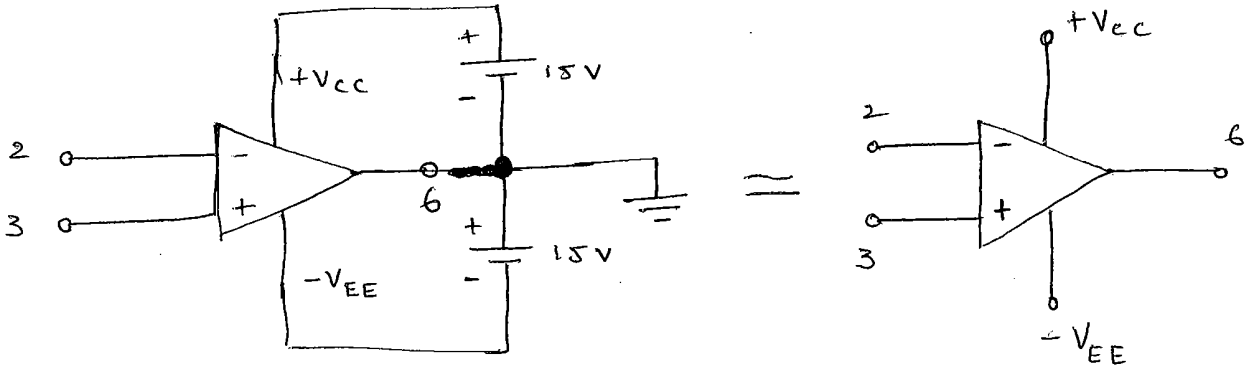
The IC 741, 8 Pin Mini DIP is shown in figure(b) below.



(b) 8-Pin Mini DIP

Power supply connections:

The $+V_{CC}$ and $-V_{EE}$ power supply terminals are connected to two dc voltage sources. The $+V_{CC}$ is connected to the positive terminal of one source and $-V_{EE}$ is connected to the negative terminal of other source. where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about ± 5 V to ± 22 V. The common terminal of $+V_{CC}$ and $-V_{EE}$ is connected to a reference point or ground.

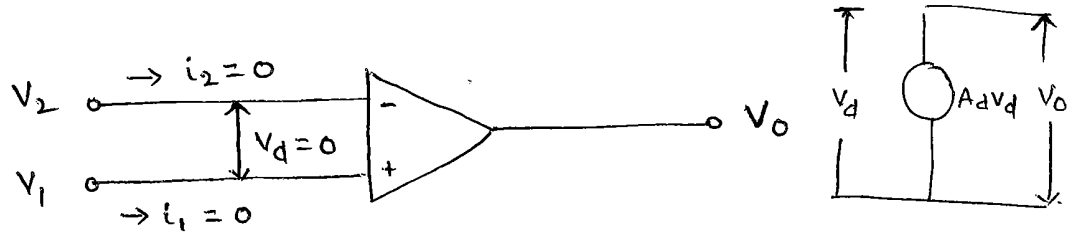


The Ideal operational Amplifier:

The schematic symbol of an op-Amp is shown in figure below. The - and + symbols at the input refer to inverting and non inverting input terminals respectively.

ie if $V_1 = 0$, output V_o is 180° out of phase with input signal V_2.

And when $V_2 = 0$. output V_o will be inphase with the input signal applied at V_1.



Fig(a): Ideal op-Amp

The op-Amp is said to be ideal if it has the following characteristics.

1. Infinite voltage gain $A_{OL} = \infty$

Since gain is ∞, the voltage between the inverting and non inverting terminals ie differential input voltage $V_d = V_1 - V_2$ is essentially zero for finite output voltage V_o.

$$A_{OL} = \frac{V_o}{V_d} = \infty \quad \Rightarrow \quad V_d = 0 = V_1 - V_2$$

2. Infinite input resistance $(R_i = \infty)$:

Because of infinite input resistance the ideal op-Amp draws no current at both the input terminals ie. $i_1 = i_2 = 0$. so that almost any signal source can drive it and there is no loading of the preceding stage.

3. zero output Resistance $[R_o = 0]$

so the output can drive an infinite number of other sources.

4. Infinite Band width $(BW = \infty)$

so that any frequency signal from 0 to ∞ Hz can be amplified with out attenuation

5. offset voltage $V_{of} = 0$

ie when $V_1 = V_2 = 0$, $V_o = 0$

6. common mode Rejection Ratio (CMRR) $= \infty$

7. slew rate (SR) $= \infty$

so the output voltage changes occur simultaneously with input voltage changes.

practical op-Amp [Equivalent circuit of op-Amp]:

The ideal op-Amp characteristics can never be realized in practice. There are practical op-Amps that can be made to approximate some of these characteristics using a negative feedback arrangement.

the physical Amplifier is not a ideal one so the characteristics of practical op-Amp are

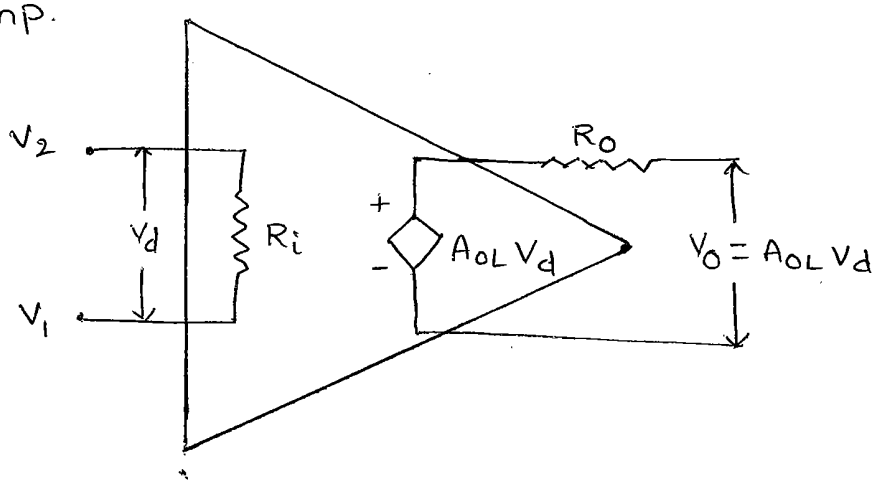
open loop voltage Gain $A_{OL} \neq \infty$

Input Impedance $R_i \neq \infty$

output Impedance $R_O \neq 0$

offset voltage V_{of} is finite if $V_1 = V_2 = 0$

Figure Below shows the equivalent circuit of an op-Amp.



For the above circuit $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_O \neq 0$. It can be seen that op-Amp voltage controlled voltage source and $A_{OL} V_d$ is an equivalent thevinin voltage Source and R_O is the thevinin equivalent resistance looking back in to the output terminal of an op-Amp.

The equivalent circuit is useful in analyzing the basic operating principles of op-Amps. For the above circuit, the output voltage is

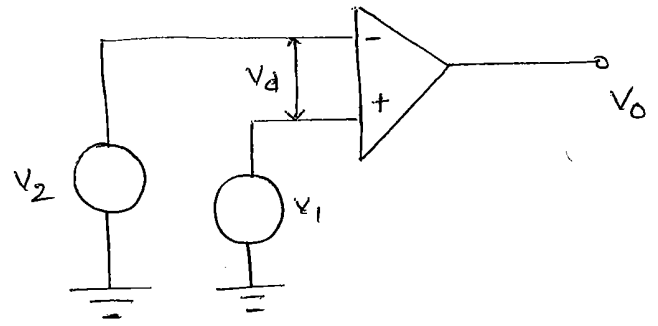
$$V_O = A_{OL} V_d$$

$$V_O = A_{OL} (V_1 - V_2)$$

The equation shows that the op-Amp amplifies the difference between the two input voltages.

open loop operation of op-Amp : (op-Amp without feedback)

The simplest way to use an op-Amp is in the open loop mode



Refer to the above figure, where signals V_1 and V_2 are applied at non inverting and inverting input terminals respectively.

Since the gain is infinite, the output voltage V_o is either at its positive saturation voltage ($+V_{sat}$) or negative saturation voltage.

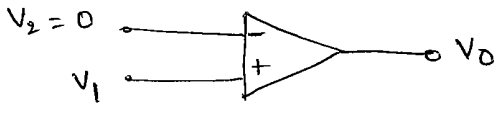
$$\text{If } V_1 > V_2 \Rightarrow V_o = +V_{sat} \simeq +V_{cc}$$

$$V_1 < V_2 \Rightarrow V_o = -V_{sat} \simeq -V_{cc}$$

Here the output assumes one of the two possible output states, that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only.

This has limited number of applications such as voltage comparator, zero Crossing detector etc. open loop op-Amps are not used in linear applications.

For practical op-Amp (open loop)



Assume $A_{OL} = 10^5$

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2)$$

$$V_o = A_{OL} V_1$$

case 1:

If $V_1 = 1\,\mu V \Rightarrow V_o = 10^5 \times 10^{-6} = 0.1\,V$

case 2:

If $V_1 = 1\,mV \Rightarrow V_o = 10^5 \times 10^{-3} = 100\,V$

Consider case (2): output voltage 100 V is not possible, because output voltage cannot be greater than supply voltage. so output is saturated

$$\text{so} \quad V_o = +V_{sat} \simeq +V_{cc}$$

similarly If $V_1 = 0$

case 1: If $V_2 = 1\,\mu V \Rightarrow V_o = -A_{OL} V_2 = -0.1\,V$

case 2: If $V_2 = 1\,mV \Rightarrow V_o = -V_{sat} \simeq -V_{cc}$.

Open loop op-Amp configurations:

There are three open loop op-Amp configurations

1. Differential Amplifier
2. Inverting Amplifier
3. Non inverting Amplifier.

1. Differential Amplifier:

Figure shows the open loop differential Amplifier in which input signals V_{in1} and V_{in2} are applied to the positive and Negative input terminals.

since the Op-Amp amplifies the difference between the two input signals, this configuration is called the differential amplifier.

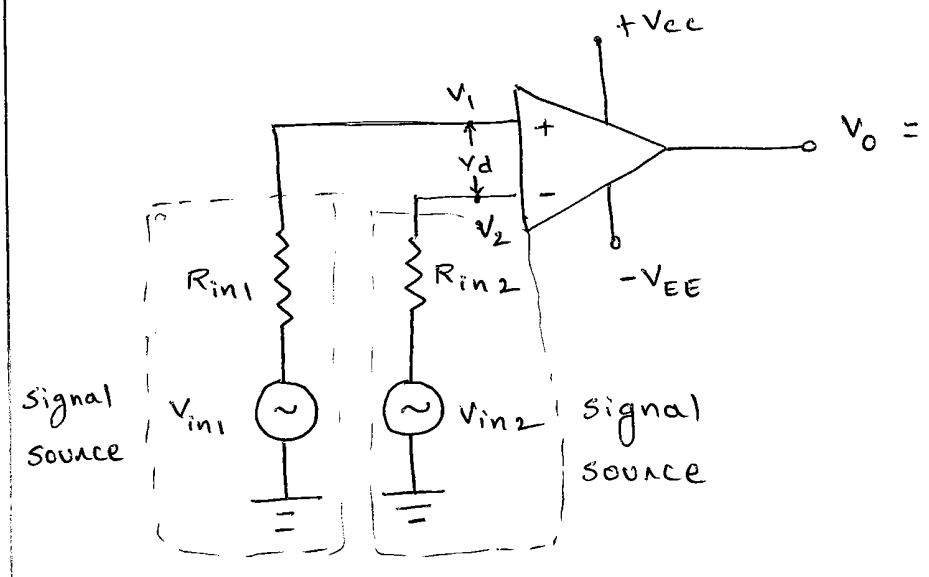


Fig: open loop differential Amplifier

$$V_o = A\, V_d$$

$$V_o = A\,(V_1 - V_2)$$

R_{in1}, R_{in2} are negligible compared to the input resistance (R_i) of the op-Amp

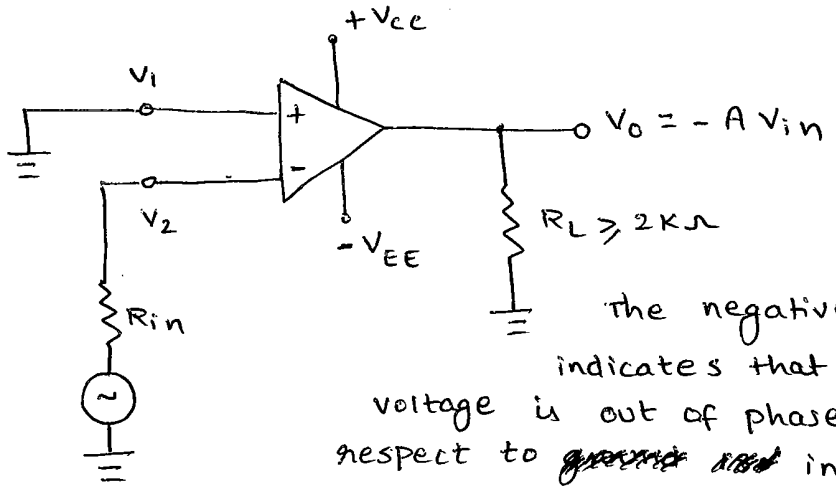
so $V_{in1} = V_1$, $V_{in2} = V_2$

$$\therefore \quad V_o = A\,(V_{in1} - V_{in2})$$

② Inverting Amplifier:

Here $V_{in} = 0$, $V_2 = V_{in}$

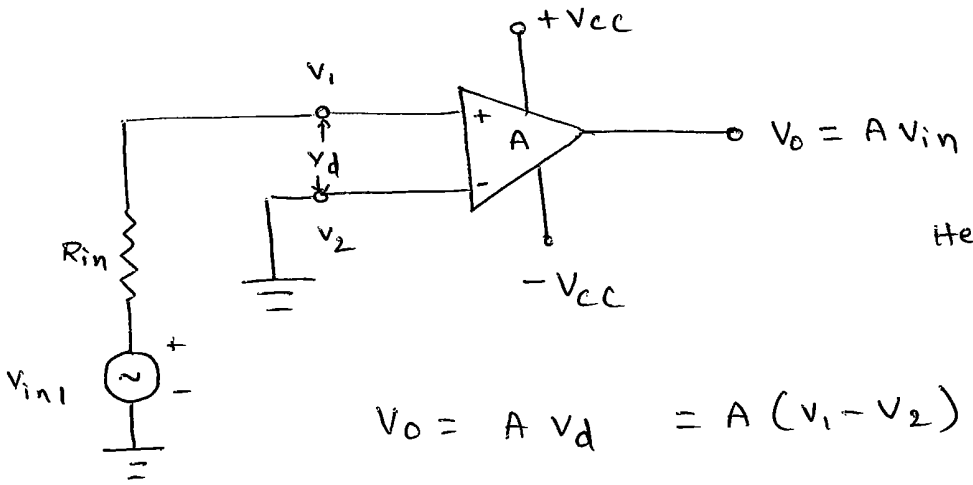
$$V_o = A\, V_d = A\,(V_1 - V_2) = -A\, V_{in}.$$



The negative sign indicates that the output voltage is out of phase with respect to input by 180°

Fig: open loop Inverting Amplifier

3) Non Inverting Amplifier:



Here $V_1 = V_{in}$

$V_2 = 0$

$$V_o = A V_d = A (V_1 - V_2)$$

$$V_o = A V_1 = A V_{in}$$

output voltage is inphase with the input voltage

Problem:

Determine the output voltage in each of the following cases for the open loop differential amplifier shown in figure above.

a) $V_{in1} = 5\mu V$ dc , $V_{in2} = -7\mu V$ dc

b) $V_{in1} = 10$ mV rms , $V_{in2} = 20$ mV rms

The op-Amp is a 741 with the following specifications : $A = 200000$, $R_i = 2M\Omega$, $R_o = 75\Omega$, $+V_{cc} = 15V$, $-V_{EE} = -15V$ and output voltage swing $= \pm 14V$.

(i) $V_o = A V_d = A (V_{in1} - V_{in2})$

$= A \{ 200000 \left(5 \times 10^{-6} - (-7) \times 10^{-6} \right)$

$= 2.4V$ dc

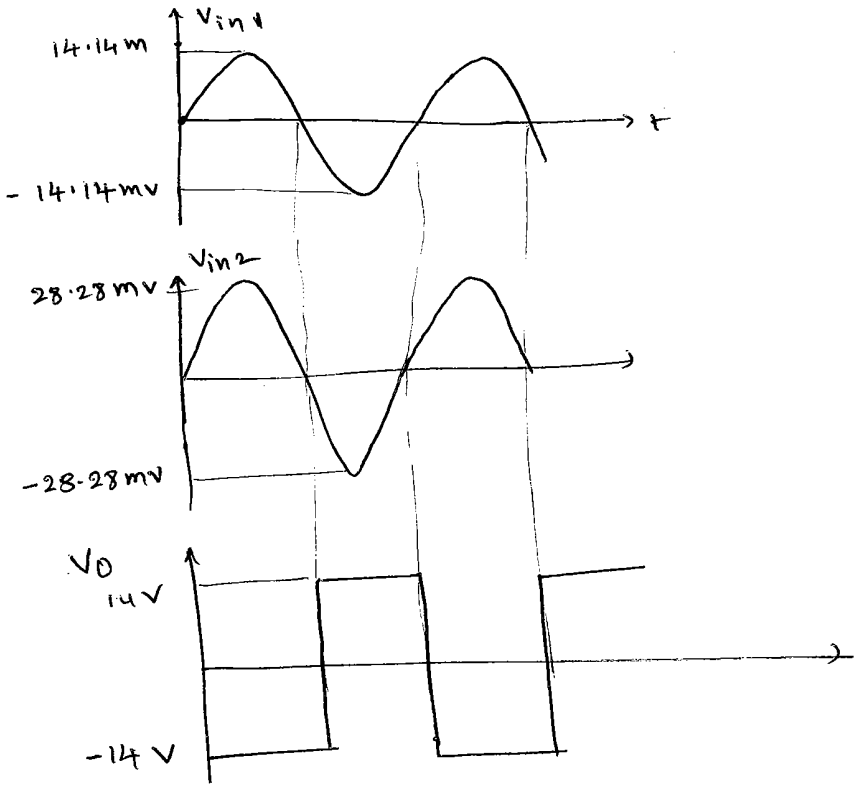
(ii) $V_o = A V_d$

$V_o = 200000 \left[10 \times 10^{-3} - (20 \times 10^{-3}) \right] = -2000 V$ rms

Now op-Amp saturates at $\pm 14V$.

$V_{in1} = 10mV$ rms $= 10\sqrt{2}$ mV $= 14.14$ mV

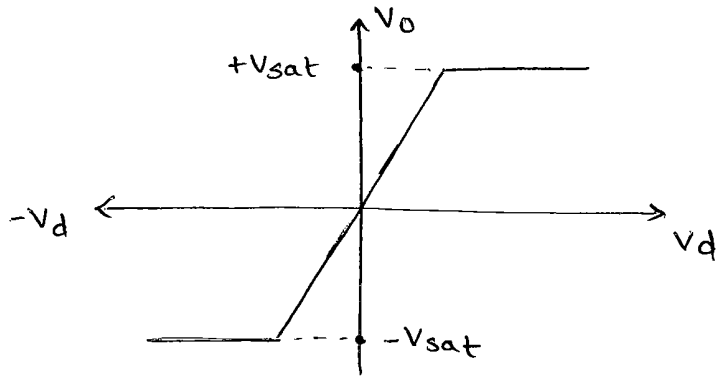
$V_{in2} = 20mV$ rms $= 20\sqrt{2}$ mV $= 28.28$ mV.



Ideal Voltage Transfer Curve :

Basic op-Amp equation $V_o = A V_d = A(V_1 - V_2)$

The plot of V_o Vs V_d is shown in figure below. keeping gain A Constant.



Here Fig: Ideal voltage transfer curve

Here Ideal because output offset voltage is assumed to be zero.

From the graph we can say that the ouput voltage is directly proportional to the input difference voltage only until it reaches the saturation voltages and that thereafter output voltage remains constant.

Feedback in Ideal op-Amp : (Negative feedback)

The utility of an op-Amp can be greatly increased by providing Negative feed back. The output in this case is not driven in to saturation and the circuit behaves in a linear manner. There are two basic feed back connections used. In order to understand the operation of these

circuits, we make two realistic simplying assumptions.

1. the current drawn by either of the input terminals (non inverting and inverting) is negligible

2. the differential input voltage V_d between non-inverting and inverting input terminals is essentially zero.

Inverting Amplifier:

The circuit of Inverting Amplifier circuit is shown in figure below.

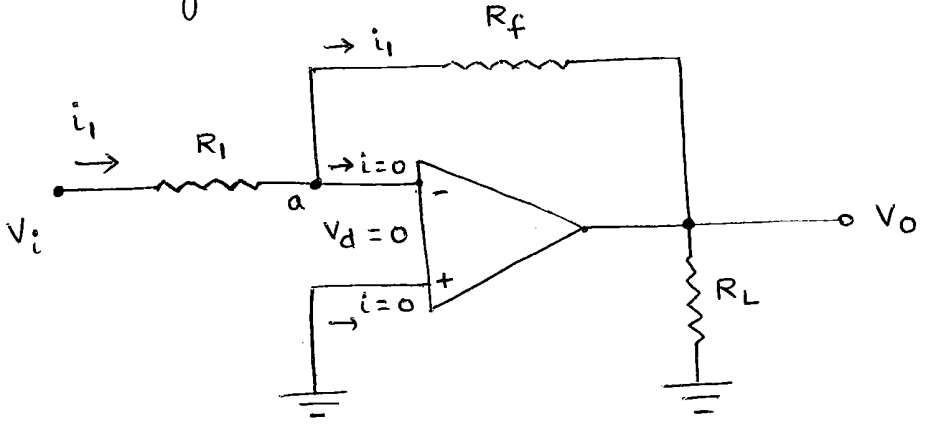


Fig: Inverting Amplifier

The output voltage V_o is fedback to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal V_i (ac or dc) is applied to the inverting input terminal through R_1 and non inverting input terminal of op-Amp is grounded.

Analysis:

For simplicity, assume an ideal op-Amp. As $V_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{V_i}{R_1} \longrightarrow (1)$$

Also since op-Amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage

From the circuit

$$i_1 = \frac{V_i - V_a}{R_1} = \frac{V_i - 0}{R_1} = \frac{V_i}{R_1} \longrightarrow (2)$$

$$i_1 = \frac{V_a - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \longrightarrow (3)$$

$(2) = (3)$ $\quad \frac{V_i}{R_1} = -\frac{V_o}{R_f} \Rightarrow A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$.

The negative sign indicates a phase shift of 180° between V_i and V_o.

Also since inverting input terminal is at virtual ground, the effective input impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect.

Problem :

Design an Amplifier with a gain of -10 and input resistance equal to 10 kΩ.

Solution:

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

The gain of inverting amplifier is $A_{CL} = \frac{-R_f}{R_1}$

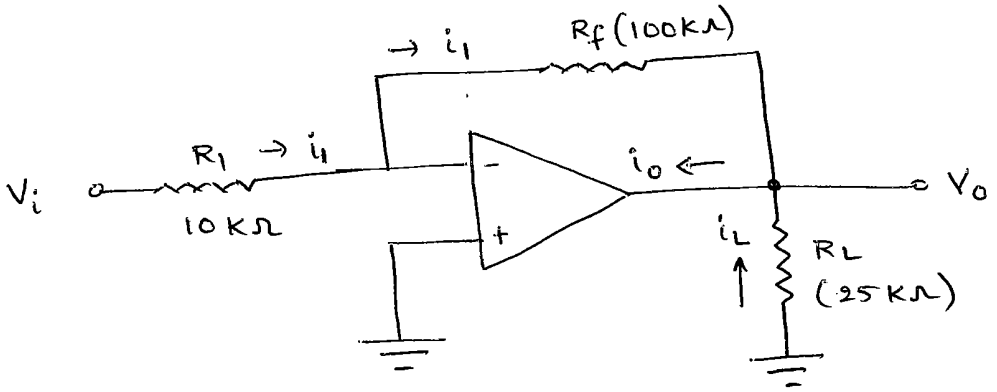
$$-10 = \frac{-R_f}{R_1} \Rightarrow$$

Choose $R_1 = 10K\Omega$

$$R_f = -A_{CL} \cdot R_1 = -(-10) \times 10K\Omega = 100K\Omega.$$

Problem:

For the circuit shown in figure below $R_1 = 10K\Omega$, $R_f = 100K\Omega$, $V_i = 1V$. A load of $25K\Omega$ is connected to the output terminal. Calculate (i) i_1 (ii) V_o (iii) i_L and total current i_o in the output pin.



Solution:

a) $$i_1 = \frac{V_i}{R_1} = \frac{1}{10K\Omega} = 0.1mA$$

b) $$V_o = \frac{-R_f}{R_1} V_i = -\frac{100K\Omega}{10K\Omega} \times 1V = -10V$$

c) $$i_L = \frac{-V_o}{R_L} = \frac{-(-10V)}{R_L} = 0.4mA.$$

d) Total current $i_o = i_1 + i_L = 0.1 + 0.4$

$$i_o = 0.5mA.$$

In an inverting amplifier, for a +ve input output will be -ve, therefore the direction of i_o is as shown in figure above

Practical Inverting Amplifier:

For a practical op-Amp the expression for the closed loop voltage gain should be calculated using the low frequency model of inverting Amplifier. The equivalent circuit of a practical inverting amplifier is shown in figure below.

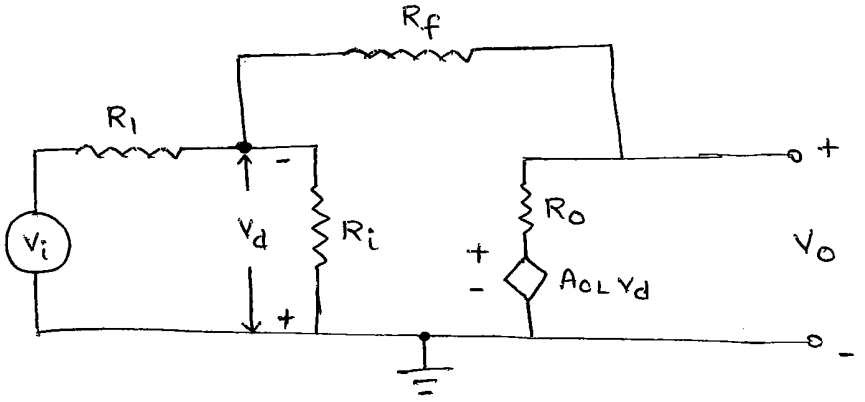
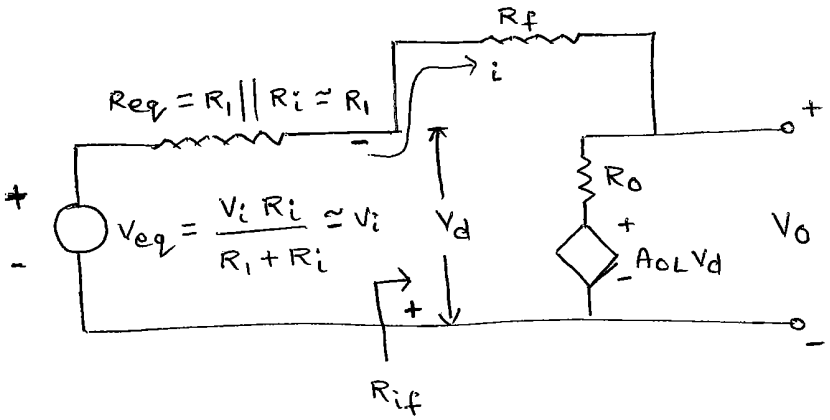


Fig: Equivalent circuit of a practical op-Amp inverting Amplifier

This circuit can be simplified by replacing the signal source V_i and resistors R_1 and R_i by thevinin's equivalent as shown in figure below, which is analysed to calculate the exact expression for closed loop gain A_{CL} and input impedance R_{if}.



Fig(b): Simplified circuit by using thevinin's Equivalent.

Fig: Simplified circuit by using thevinin's equivalent

the input impedance R_i of an op-Amp is usually much greater than R_1, so we may assume

$V_{eq} \simeq V_i$ and $R_{eq} = R_1$.

From the output loop in figure (b)

$$V_o = iR_o + A_{OL} V_d \longrightarrow (1)$$

Also $$V_d + iR_f + V_o = 0 \longrightarrow (2)$$

Putting the value of V_d from eq (2) to eq (1) and simplifying

$$V_o = iR_o + A_{OL}\left(-iR_f - V_o\right)$$

$$V_o\left(1 + A_{OL}\right) = i\left(R_o - A_{OL} R_f\right) \longrightarrow (3)$$

Also the KVL loop equation gives

$$V_i = i(R_1 + R_f) + V_o \longrightarrow (4)$$

Putting the value of i from eq (3) in eq (2) and solving for closed loop gain

$$A_{CL} = \frac{V_o}{V_i}$$

$$V_i = \frac{V_o(1 + A_{OL})}{R_o - A_{OL} R_f} (R_1 + R_f) + V_o$$

$$V_i = \frac{V_o(1 + A_{OL}) + V_o R_o - A_{OL} R_f V_o}{R_o - A_{OL} R_f}$$

$$V_i(R_o - A_{OL} R_f) = V_o(R_o$$

$$V_i\left(R_o - A_{OL} R_f\right) = V_o\left(1 + A_{OL}\right)(R_1 + R_f) + V_o R_o - V_o A_{OL} R_f$$

$$V_i\left(R_o - A_{OL} R_f\right) = V_o R_1 + V_o R_f + V_o A_{OL} R_1 + V_o A_{OL} R_f + V_o R_o - V_o A_{OL} R_f$$

$$V_i\left(R_0 - A_{OL}R_f\right) = V_0\left(R_0 + R_f + R_1\left(1+A_{OL}\right)\right]$$

$$A_{CL} = \frac{V_0}{V_i} = \frac{R_0 - A_{OL}R_f}{R_0 + R_f + R_1\left(1+A_{OL}\right)}$$

[If $A_{OL} >> 1$,

$$A_{CL} = \frac{R_0 - A_{OL}R_f}{R_0 + R_f + A_{OL}R_1}$$ and $A_{OL}R_1 >> R_0 + R_f$, $R_0 = 0$

$$A_{CL} = \frac{-R_f}{R_1}$$]

Input Resistance R_{if} :— From fig(b)

$$R_{if} = \frac{V_d}{i}$$

writing the loop equation and solving for R_{if}

$$V_d + i\left(R_f + R_0\right) + A_{OL}V_d = 0$$

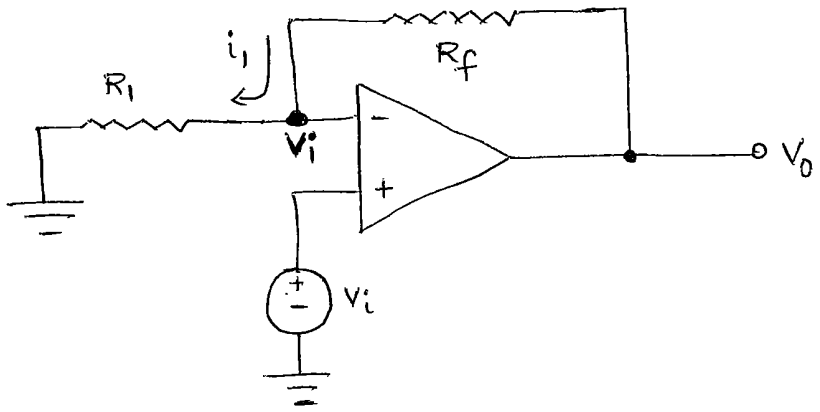
$$V_d\left(1+A_{OL}\right) = -\left(R_f + R_0\right)i$$

$$\therefore R_{if} = \frac{V_d}{i} = \frac{-\left(R_f + R_0\right)}{1 + A_{OL}}$$

Non inverting Amplifier:

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given as shown in figure below.

the circuit amplifies with out inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as feed back is being fed back to the inverting input terminal.



$$i_1 = \frac{V_0 - V_i}{R_f} \longrightarrow (1)$$

$$i_1 = \frac{V_i}{R_1} \longrightarrow (2)$$

$$\frac{V_0 - V_i}{R_f} = \frac{V_i}{R_1} \Rightarrow \frac{V_0}{R_f} = V_i\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\Rightarrow \frac{V_0}{V_i} = R_f\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$A_{CL} = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Problem: Design an Amplifier with a gain of +5 using one OP-Amp.

Solution: Since the gain is positive, the amplifier is Non-inverting Amplifier.

Assume $R_1 = 10K\Omega$

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

$$5 = 1 + \frac{R_f}{R_1} \Rightarrow R_f = 4R_1$$

$$R_f = 4 \times 10K\Omega = 40K\Omega.$$

problem: In the circuit shown in figure below let $R_1 = 5K\Omega$, $R_f = 20K\Omega$ and $V_i = 1V$. A load resistor of $5K\Omega$ is connected at the output. calculate

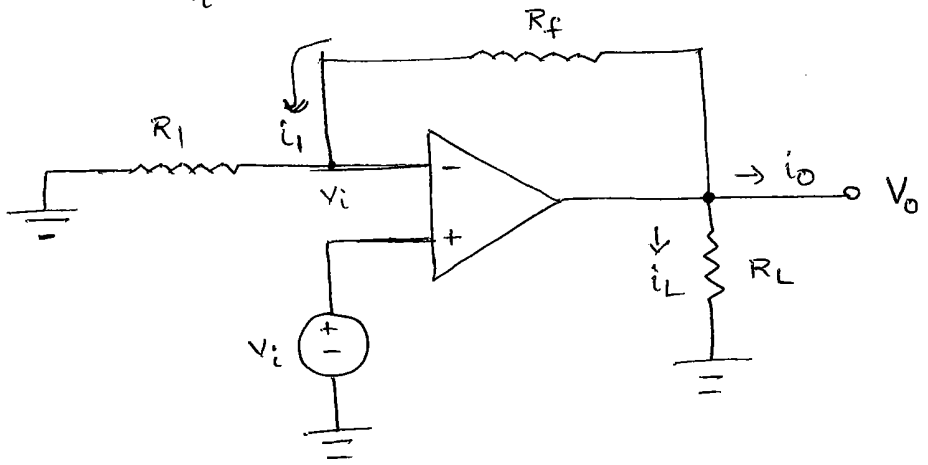
(i) V_o (ii) A_{CL} (iii) the load current i_L (iv) the output current i_o indicating proper direction of flow.

Solution:

(i) $$V_o = \left(1 + \frac{R_f}{R_1}\right) V_i = \left(1 + \frac{20K\Omega}{5K\Omega}\right)(1V) = 5V$$

(ii) $$A_{CL} = \frac{V_o}{V_i} = \frac{5V}{1V} = 5$$

(iii)



(iii) $$i_L = \frac{V_o}{R_L} = \frac{5}{5K\Omega} = 1mA$$

(iv) $$i_1 = \frac{V_i}{R_1} = \frac{1}{5K\Omega} = 0.2mA$$

(iv) $$i_o = i_L + i_1 = 1mA + 0.2mA = 1.2mA$$

The op-Amp output current i_o flows outwards from the output junction.

Practical Non-Inverting Amplifier:

The analysis of practical non-inverting Amplifier can be performed by using the equivalent circuit shown in figure below.

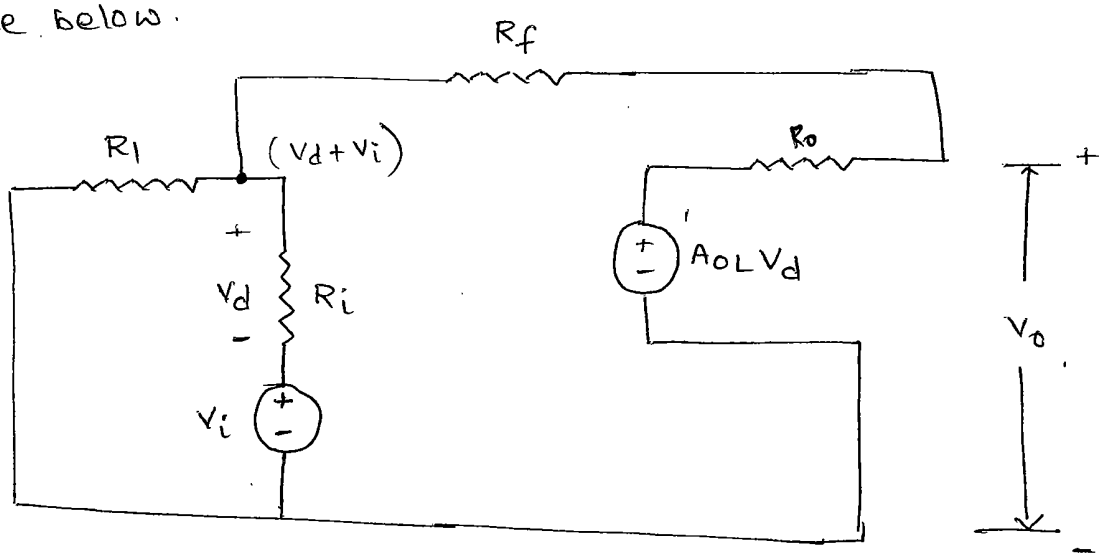


Fig: Equivalent circuit of Non inverting Amplifier using Low frequency model.

writing KCL at the input node

$$\left(V_o - (V_d + V_i)\right) Y_f = (V_d + V_i) Y_i + V_d Y_i$$

$$Y_f V_o = V_d (Y_i + Y_i + Y_f) + V_i (Y_i + Y_f) \longrightarrow (1)$$

writing KCL at the output node

$$(V_d + V_i - V_o) Y_f = (V_o - A_{OL} V_d) Y_o$$

$$V_o (Y_f + Y_o) = V_d (A_{OL} Y_o + Y_f) + Y_f V_i \longrightarrow (2)$$

From Eq (1) $$V_d = \frac{Y_f V_o - (Y_i + Y_f) V_i}{Y_i + Y_i + Y_f} \longrightarrow (3)$$

Substitute Eq (3) in Eq (2), After simplifying

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{OL}\, Y_0 (Y_1 + Y_f) - Y_f Y_i}{(A_{OL} - 1) Y_0 Y_f - (Y_1 + Y_i)(Y_0 + Y_f)} \longrightarrow (4)$$

This is the required closed loop gain of practical non inverting Amplifier.

[For Ideal Amplifier, $A_{OL} \longrightarrow \infty$, so using in Eq (4), we get

$$A_{CL} = \frac{A_{OL}\, Y_0 (Y_1 + Y_f) - \frac{Y_f Y_i}{A_{OL}}}{(Y_0 \cdot Y_f) - \frac{Y_0 Y_f}{A_{OL}} - \frac{(Y_1 + Y_i)(Y_0 + Y_f)}{A_{OL}}} \Bigg|_{A_{OL} \to \infty}$$

$$A_{CL} = \frac{Y_0 (Y_1 + Y_f)}{Y_0 Y_f} = 1 + \frac{Y_1}{Y_f} \simeq 1 + \frac{R_f}{R_1}$$

Virtual Ground :

The differential input voltage V_d between the non inverting and inverting terminals is essentially zero.

This is obvious because even if output voltage is few volts, due to large open loop gain of op-Amp, the difference voltage V_d at the input terminals is almost zero.

Ex of output voltage is 10V and the A_{OL} is 10^4 then

$$V_o = V_d . A_{OL}$$

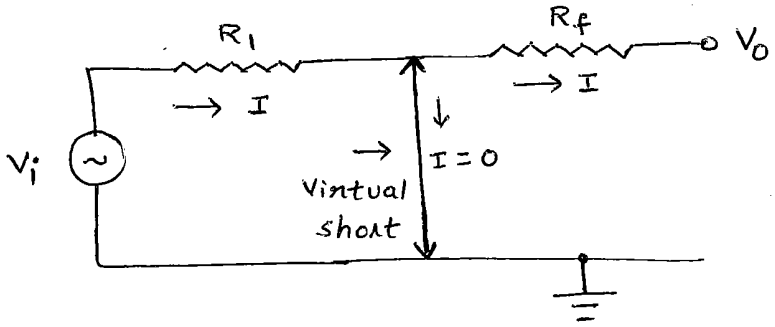
$$V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1mV$$

Hence V_d is very small.

As $A_{OL} \to \infty$, the differential voltage $V_d \to 0$, and assumed to be zero for analysing the circuits.

$$V_d = \frac{V_o}{A_{OL}} \Rightarrow V_1 - V_2 = \frac{V_o}{A_{OL}} = \frac{V_o}{\infty} = 0$$

$$V_1 = V_2$$



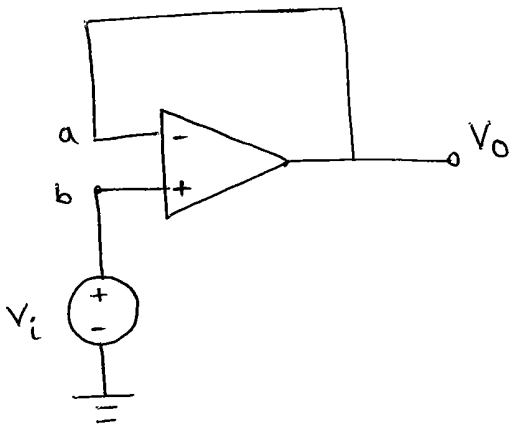
Thus we can say that under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same. No current flows from input terminals to the ground.

The above figure shows that the concept of virtual ground. The thick line indicates the virtual short between the input terminals.

Now if the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. This is the principle of virtual ground.

Voltage Follower:

In the Non-inverting amplifier if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit shown in figure below



Here $V_b = V_i$ and $V_a = V_b$

$\therefore V_a = V_i$

Now $V_o = V_a$ and $\boxed{V_o = V_i}$

That is the output voltage is equal to input voltage both in magnitude and phase. In other words we can say that the output voltage follows the input voltage exactly. Hence the circuit is called a 'Voltage Follower'.

It is also called buffer Amplifier, unity gain amplifier and isolation Amplifier.

Advantages:

1- Input impedance is very high (ie $M\Omega$), low output impedance. therefore it draws negligible current from the source. Thus a voltage follower

may be used as buffer for impedance matching that is, to connect a high impedance source to a low impedance load.

2. It has large bandwidth

Differential Amplifier :

A circuit that Amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits.

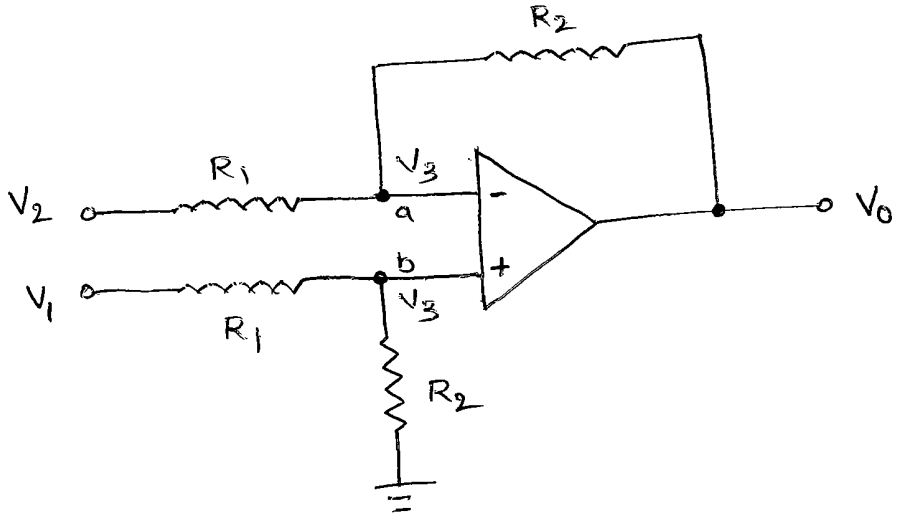


Fig : Differential Amplifier

$$\frac{V_2 - V_3}{R_1} = \frac{V_3 - V_0}{R_2}$$

and $$\frac{V_1 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 = \frac{V_1}{R_1}$$

After simplifying

$$V_0 = \frac{R_2}{R_1}(V_1 - V_2)$$

Such a circuit is very useful in detecting very small differences in signals. since the gain $\frac{R_2}{R_1}$ can be chosen to be very large For example if $R_2 = 100 R_1$, then a small difference $V_1 - V_2$ is amplified 100 times.

Difference mode and common mode Gains.

output of a differential amplifier

$$V_0 = \frac{R_2}{R_1}(V_1 - V_2) \longrightarrow (1)$$

If $V_1 = V_2$ then $V_0 = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-Amp, however a practical op-Amp exhibits some small response to the common mode component of the input voltages too.

For example, the output V_0 will have different value for cases

(i) with $V_1 = 100\mu V$ and $V_2 = 50\mu V$

(ii) with $V_1 = 1000\mu V$ and $V_2 = 950\mu V$

even though the difference signal $V_1 - V_2 = 50\,\mu V$ in both the cases.

the output voltage depends not only upon the difference signal V_d at the input, but is also affected by the average voltage of the input signals, called the common-mode signal V_{CM} defined as

$$V_{CM} = \frac{V_1 + V_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So even with the same voltage applied to both inputs, the output is not zero. The output therefore must be expressed as

$$V_o = A_1 V_1 + A_2 V_2 \longrightarrow (2)$$

where V_1 = voltage multiplication from input 1 to the output with input 2 grounded

V_2 = voltage multiplication from input 2 to the output with input 1 grounded.

since $V_{cm} = \frac{V_1 + V_2}{2}$ and $V_d = (V_1 - V_2)$

$$V_1 = V_{cm} + \frac{1}{2} V_d \longrightarrow (3)$$

$$V_2 = V_{CM} - \frac{1}{2} V_d \longrightarrow (4)$$

Substitute the value of V_1 and V_2 in eq ②, we get

$$V_o = A_{DM} V_d + A_{CM} V_{CM} \longrightarrow ④$$

where $A_{DM} = \frac{1}{2}(A_1 - A_2)$

$$A_{CM} = A_1 + A_2$$

The voltage gain for the difference signal is A_{DM} and that for the common mode signal is A_{CM}

Common mode Rejection Ratio :

The relative sensitivity of an op-Amp to a difference signal as compared to a common mode signal is called common mode Rejection Ratio (CMRR) and gives the figure of merit (ρ) for the differential amplifier. So, CMRR is given by

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right|$$

and is usually expressed in decibels (dB)

For example, the μA741 op-Amp has a minimum CMRR of 70 dB.

we should have A_{DM} large, A_{CM} should be zero ideally. So, higher the value of CMRR, better is the op-Amp.

Problem:

Determine the output of a differential amplifier for the input voltages of 300μv and 240μv. The differential gain of the amplifier is 5000 and the value of CMRR is (i) 100 (ii) 10^5.

Solution:

case 1: $CMRR = 100$, $V_1 = 300\mu V$, $V_2 = 240\mu V$

$$V_d = V_1 - V_2 = 300\mu V - 240\mu V = 60\mu V$$

$$V_{CM} = \frac{V_1 + V_2}{2} = \frac{300\mu V + 240\mu V}{2} = 270\mu V$$

$$A_{DM} = 5000$$

$$CMRR = \frac{A_{DM}}{A_{CM}} \Rightarrow A_{CM} = \frac{A_{DM}}{CMRR} = \frac{5000}{100}$$

$$\Rightarrow A_{CM} = 50$$

$$V_0 = A_{DM} V_d + A_{CM} V_{CM}$$

$$V_0 = (5000 \times 60\mu V) + (50 \times 270\mu V)$$

$$V_0 = 313.5 mV.$$

case 2: $CMRR = 10^5$, $V_1 = 300\mu V$, $V_2 = 240\mu V$

$$CMRR = \frac{A_{DM}}{A_{CM}} \Rightarrow A_{CM} = \frac{A_{DM}}{CMRR} = \frac{5000}{10^5} =$$

$$V_0 = 300.0135 mV.$$

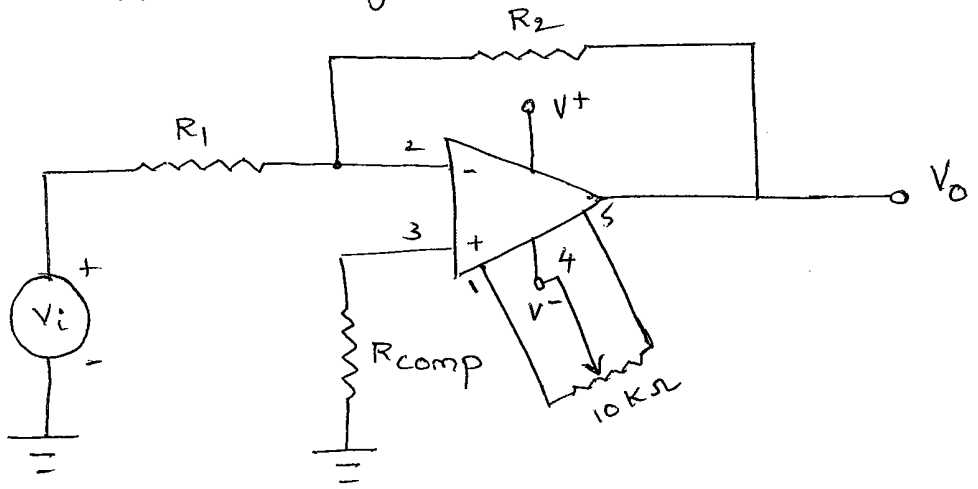
used, is given by

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

However with R_{comp} in the circuit then

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os}$$

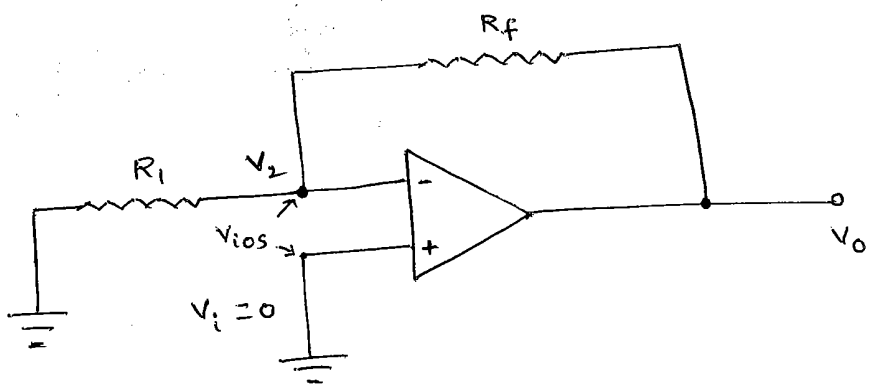
Many OP-Amps provide offset compensation pins to nullify the offset voltage. Figure below gives the connections for the 741 OP-Amp. The manufacturers recommend that a 10kΩ potentiometer ~~potentiometer~~ be placed across offset null pins 1 and 5 and the wiper be connected to the negative supply pin 4. The position of the wiper is adjusted to nullify the output offset voltage.



Thermal Drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°c may not remain so when the temperature rises to 35°c. This is called drift.

offset current drift is expressed in nA/°c and offset voltage drift in mv/°c. These indicate the change in offset for each degree celcius change in temperature.



The voltage V_2 at the inverting terminal is

$$V_2 = V_o \frac{R_1}{R_1 + R_f}$$

$$\Rightarrow V_o = V_2 \left(\frac{R_1 + R_f}{R_1} \right) = \left(1 + \frac{R_f}{R_1} \right) V_2$$

Since $V_{ios} = |V_i - V_2|$ and $V_i = 0$

$$V_{ios} = |0 - V_2| = V_2$$

$$V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

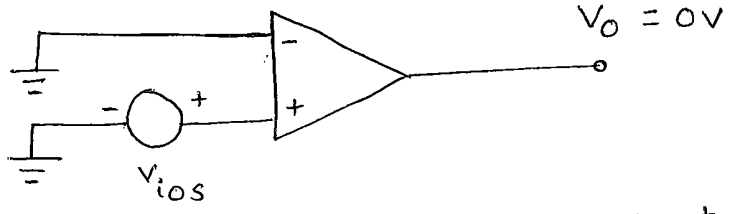
Thus the output offset voltage of an op-Amp in closed loop configuration is given by above eq.

Total output offset voltage:

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current or input offset voltage alone. this is because input offset voltage V_{ios} and the input bias current I_B could be either positive or negative with respect to ground. Therefore the max offset voltage at the output of an inverting and non inverting amplifier without any compensating technique

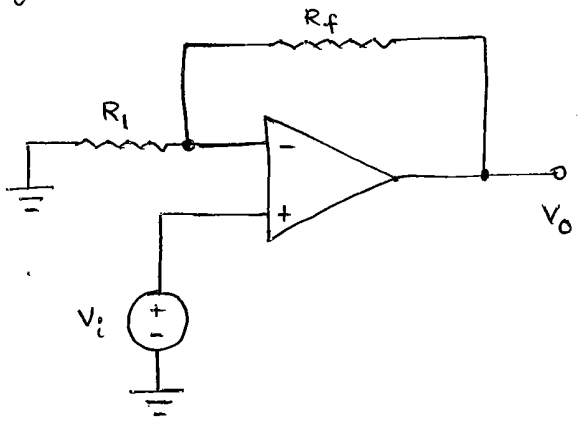
Input offset voltage :

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-Amp and a small voltage is to be applied ~~at~~ Bln the input terminals to make output voltage zero. This voltage is called Input offset voltage V_{ios}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in figure below.

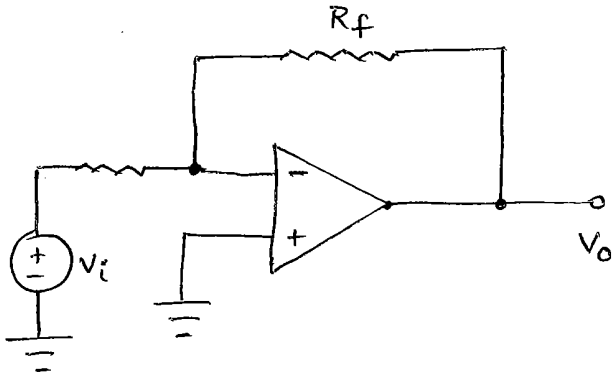


Fig(a): op-Amp showing input offset voltage.

Figure shows the Non-inverting and Inverting Amplifier CKts



Fig(b): Non Inverting Amplifier



Fig(c): Inverting Amplifier

If V_i is set to zero, the above circuits become the same as shown in figure below.

To obtain high input resistance R_1 must be kept large. with R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

the T- feedback network is a good solution. This will allow large feedback resistance while keeping the resistance to ground (seen by the inverting i/p) low as shown in the dotted lines.

The T- network provides a feedback signal as if the network were a single feedback resistor

By T to π Conversion

$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}.$$

To design a T- network, first pick $R_t << \frac{R_f}{2}$ then calculate $R_s = \frac{R_t^2}{R_f - 2R_t}$.

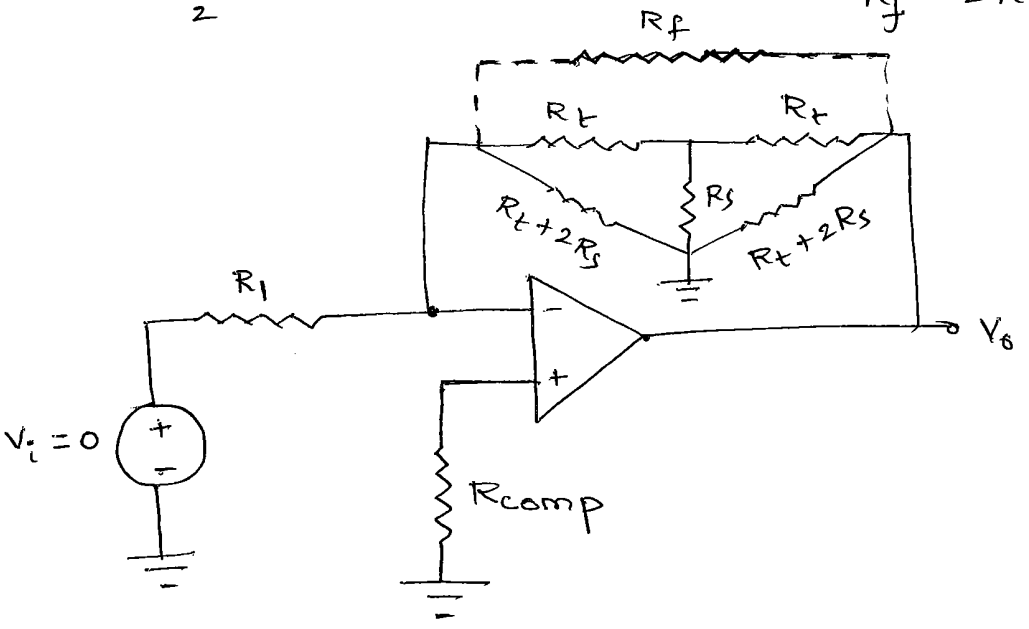


Fig: Inverting Amplifier with T- feedback Network

KCL at node 'a' gives

$$I_B^- = I_1 + I_2 \Rightarrow I_2 = I_B^- - I_1$$

$$I_2 = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right) \rightarrow (4)$$

Again $$I_2 = \frac{V_0 + V_1}{R_f} \Rightarrow V_0 = I_2 R_f - V_1$$

$$V_0 = I_2 R_f - I_B^+ (R_{comp})$$

$$\Rightarrow V_0 = \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp}$$

$$V_0 = \left(I_B^- R_f - \left(I_B^+ \left(R_{comp} \frac{R_f}{R_1} + R_{comp} \right) \right) \right)$$

$$V_0 = I_B^- R_f - I_B^+ R_{comp} \left(1 + \frac{R_f}{R_1} \right)$$

$$V_0 = I_B^- R_f - I_B^+ \frac{R_f R_1}{R_f + R_1} \left(\frac{R_f + R_1}{R_1} \right)$$

$$V_0 = R_f \left(I_B^- - I_B^+ \right)$$

$$V_0 = R_f I_{os} . \rightarrow (5)$$

So even with bias current compensation and with the feedback resistor of 1MΩ, a 741 BJT op-Amp has an output offset voltage

$V_0 = 1M\Omega \times 200nA = 200mV$. with a zero input voltage.

From it can be seen from Equation (5) that the effect of offset current can be minimized by keeping R_f small

Input offset Current :

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. The difference is called the offset current I_{os} and can be written as

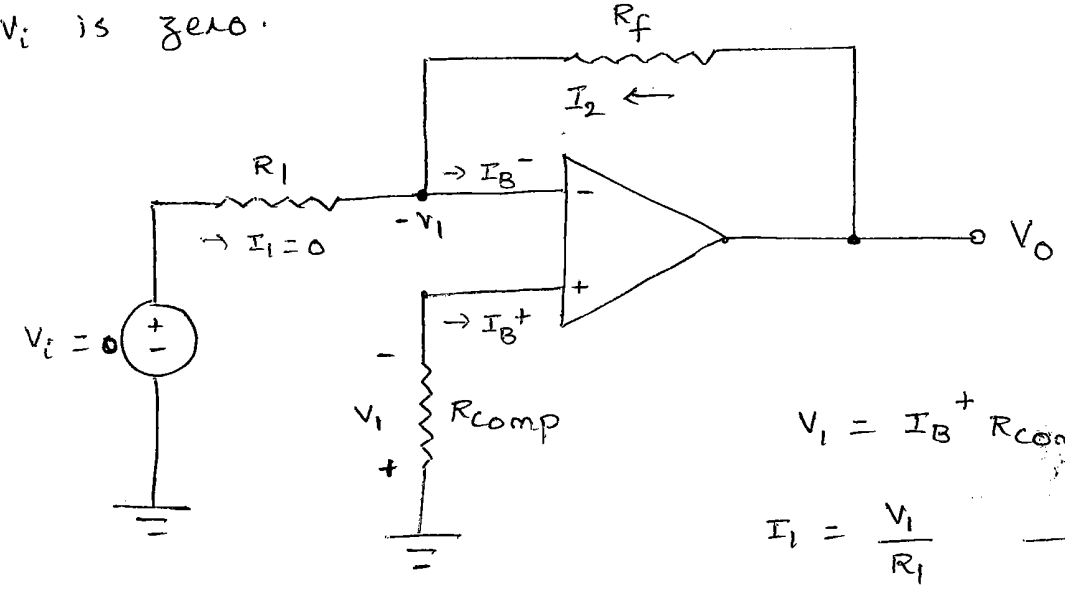
$$|I_{os}| = I_B^+ - I_B^-$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT Op-Amp is 200nA

FET Op-Amp is 10pA.

Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero.



$$V_1 = I_B^+ R_{comp} \longrightarrow (1)$$

$$I_1 = \frac{V_1}{R_1} \longrightarrow (2)$$

$$I_1 = I_B^+ \left(\frac{R_{comp}}{R_1}\right) \longrightarrow (3)$$

KCL at node a

For compensation V_o should be zero for $V_i = 0$, that is from Eq ① $V_2 = V_1$

so that $I_2 = \frac{V_1}{R_f}$

KCL at node 'a' gives $I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1}$

Assuming $I_B^- = I_B^+$

$$V_1\left[\frac{1}{R_f} + \frac{1}{R_1}\right] = I_B^+$$

From Eq ②

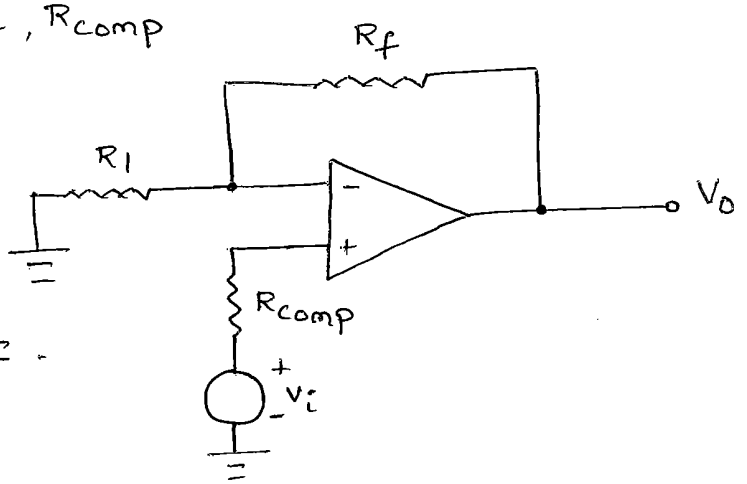
$$V_1\left[\frac{1}{R_f} + \frac{1}{R_1}\right] = \frac{V_1}{R_{comp}}$$

$$\Rightarrow \frac{1}{R_{comp}} = \frac{1}{R_f} + \frac{1}{R_1}$$

$$\Rightarrow R_{comp} = R_1 \| R_f$$

That is to compensate for bias currents, the corresponding resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

The effect of input bias current in a non-inverting amplifier can also be compensated by placing a compensating resistor, R_{comp} in series with the input signal V_i as shown in figure



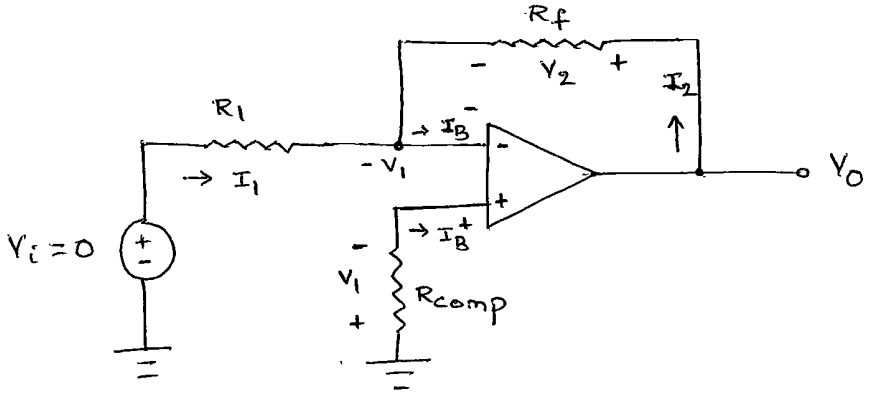
Here $R_{comp} = R_1 \| R_f$.

For example, For a 741 op-Amp, with a $R_f = 1M\Omega$

$$V_o = I_B^- R_f = 500\,nA \times 1M\Omega = 500\,mV$$

with zero input, because of bias currents, the output is driven to 500mV

This Effect can be compensated for as shown in fig(c) where a compensation resistor R_{comp} has been added between the non-inverting terminal and ground.



current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then by KVL we get

$$V_o = V_2 - V_1 \longrightarrow (1)$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. the value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}} \longrightarrow (2)$$

Now $V_a = -V_1 \Rightarrow$ $I_1 = \frac{V_a - (-V_1)}{R_1} = \frac{0 + V_1}{R_1} = \frac{V_1}{R_1}$

Also $I_2 = \frac{V_2}{R_f}$

Even though both the transistors are identical, I_B^- and I_B^+ are not equal due to internal imbalances between the two inputs.

Manufacturers specify input bias current I_B as the average value of the base currents entering in to the terminals of an op-Amp.

$$\text{so} \quad I_B = \frac{I_B^+ + I_B^-}{2}$$

For 741 (BJT) op Amp $\rightarrow I_B = 500\,nA \quad (I_B^+ = I_B^- = 500\,nA)$

For FET op-Amp $\rightarrow I_B = 50\,pA$.

Consider the basic inverting Amplifier

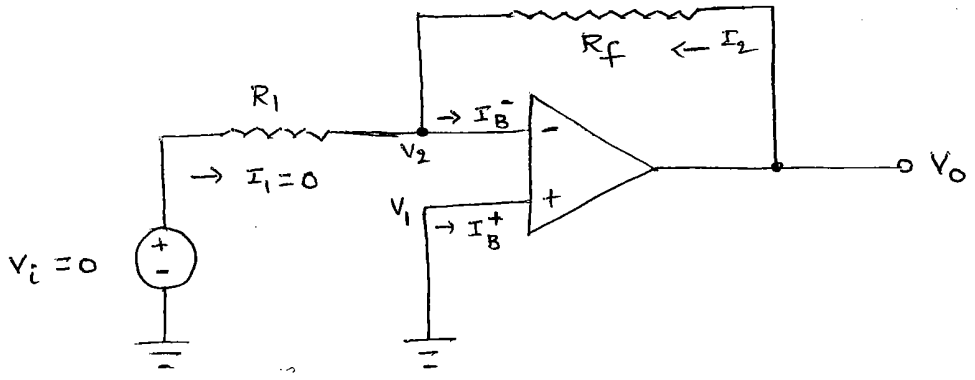


Fig (b): Inverting Amplifier with bias currents

If the input voltage $V_i = 0$, V_o should also be zero Instead the output voltage is offset by

From the ckt $\quad I_1 + I_2 = I_B^-$

$$I_1 = 0 \Rightarrow I_2 = I_B^-$$

$$I_2 = \frac{V_o - V_2}{R_f} = I_B^-$$

$$V_o - 0 = I_B^- R_f \Rightarrow V_o = I_B^- R_f$$

Operational Amplifier characteristics

DC Characteristics: An ideal op-Amp draws no current from the source and its response is also independent of temperature. However a real op-Amp doesn't work this way. Current is taken from the source in to the op-Amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-Amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage are

1) Input Bias Current
2) Input offset Current
3) Input offset Voltage
4) Thermal Drift.

1) Input Bias Current:

Practically input terminals conduct a small value of dc current to bias the input transistors. The base currents entering in to the inverting and non inverting terminals are shown as I_B^- and I_B^+ respectively. (Fig (a))

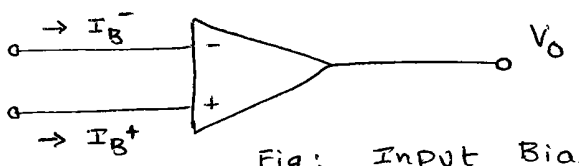


Fig: Input Bias Currents

there are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-Amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

problem:

a) For the non-inverting amplifier if $R_1 = 1k\Omega$ and $R_f = 10k\Omega$. Calculate the maximum output offset voltage due to V_{ios} and I_B. the op-Amp is LM307 with $V_{ios} = 10mV$ and $I_B = 300nA$, $I_{os} = 50nA$.

b) calculate the value of R_{comp} needed to reduce the effect of I_B

c) calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit

solution:

a) $$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

$$V_{OT} = \left(1 + \frac{10k\Omega}{1k\Omega}\right)(10\,mV) + (10k\Omega)(300nA) = 113\,mV$$

b) The value of R_{comp} needed is

$$R_{comp} = 1k\Omega \,||\, 10k\Omega = 990\Omega$$

c) with R_{comp} in the circuit

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os} = 110\,mV + 0.5\,mV$$

$$V_{OT} = 110.5\,mV.$$

problem:

A non inverting Amplifier with a gain of 100 is nulled at 25°c. what will happen to the output voltage if the temperature rises to 50°c for an offset voltage drift of 0.15mv/°c ?

solution:

Input offset voltage due to temperature rise

$$V_{ios} = 0.15\,mV/^{\circ}C \times (50^{\circ}C - 25^{\circ}C) = 3.75\,mV.$$

since this is an input change, the output voltage will change by

$$V_o = V_{ios} \times A_{CL}$$

$$V_o = 3.75\,mV \times 100 = 375\,mV.$$

AC characteristics:

1. Frequency Response:

Ideally an op-Amp should have an infinite bandwidth. the practical op-Amp gain, however decreases at higher frequencies, because of the capacitive component in the equivalent circuit of the op-Amp.

Two major sources are responsible for capacitive effects

1. physical characteristics of semi conductor devices; opAmps are composed of BJT's and FET's which contain junction capacitors. As frequency increases, the reactance of these capacitors decrease
2. The Internal Construction of the op-Amp is a second source of capacitive effects. In op-Amps a number of transistors as well as resistors and some times a capacitor are integrated on the same material, called a substrate. Infact, the substrate acts as an insulator and helps to separate these components. the various components are connected by conducting paths, and the paths are separated by insulators. However, whenever two conducting paths are separated by an insulator, it acts as a capacitor. this means that because of its construction the op-Amp may contain a number of such stray capacitors.

The cumulative effect of these capacitors due to the characteristics of semi conductor devices and the internal construction of the op-Amp causes the gain to decrease as the frequency increases.

For an op-Amp with only one break frequency, we will represent all the capacitive effects by a single capacitor as shown in figure below.

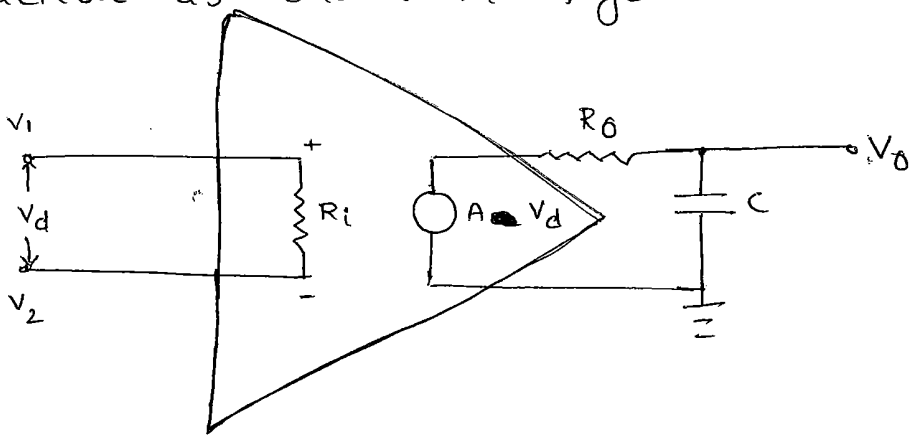


Fig: High frequency model of an op-Amp with single break frequency.

The gain as a function of frequency can be obtained as

$$V_o = \frac{-jX_c}{R_o - jX_c} A V_d$$

$$V_o = \frac{\frac{1}{j2\pi f C}}{R_o + \frac{1}{j2\pi f C}} A V_d$$

$$V_o = \frac{A V_d}{1 + j2\pi f R_o C}$$

Hence the open loop voltage gain is

$$A_{OL}(f) = \frac{V_o}{V_d}$$

$$A_{OL}(f) = \frac{A}{1 + j2\pi f R_o C}$$

Let $f_o = \frac{1}{2\pi R_o C}$, then

$$A_{OL}(f) = \frac{A}{1 + j\left(\frac{f}{f_o}\right)}$$

where $A_{OL}(f)$ = open loop voltage gain as a function of frequency

A = Gain of the op-Amp at 0 Hz (dc)

f = operating frequency

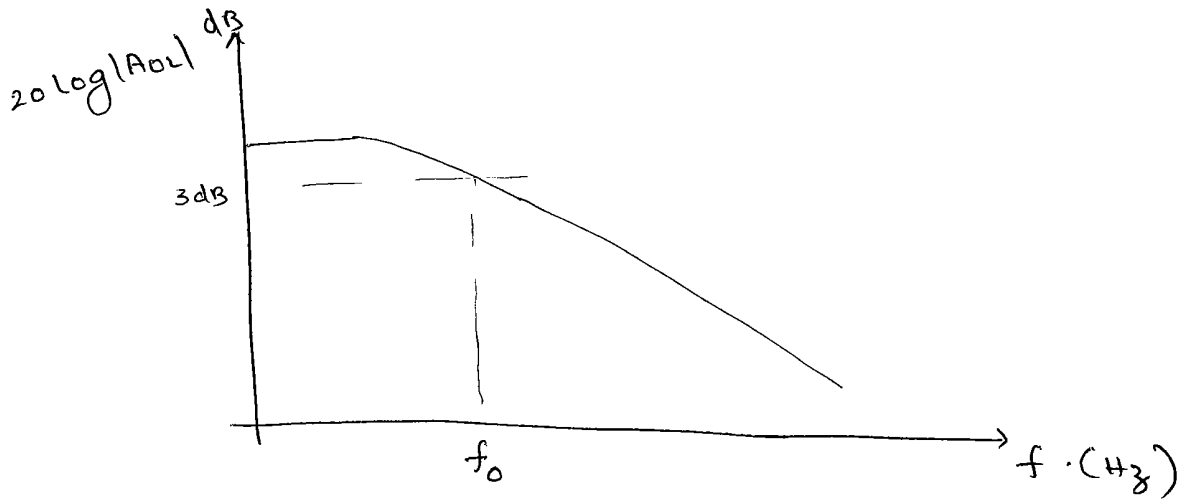
f_o = break frequency of the op-Amp.

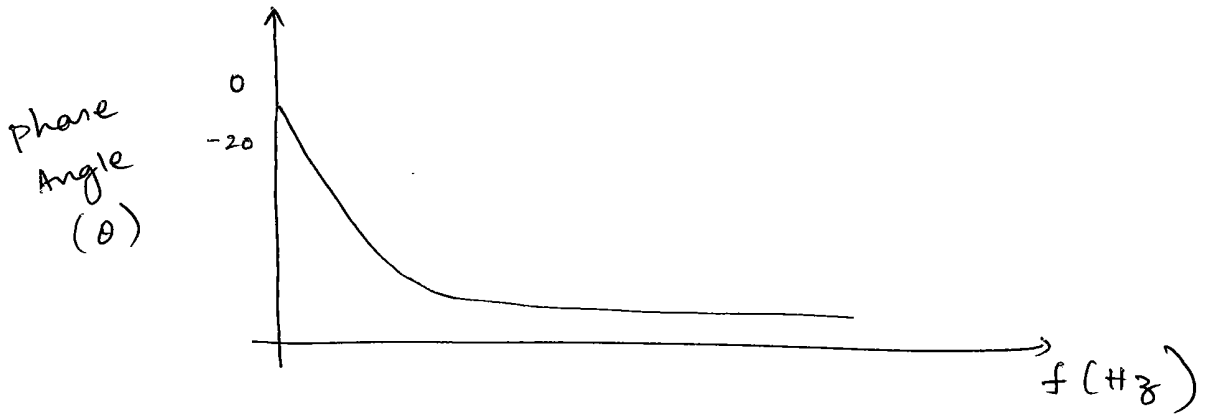
Now the break frequency f_o depends on the value of C and on output resistance R_o. Therefore f_o is fixed for a given op-Amp.

$$|A_{OL}(f)| = \frac{A}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}} \quad \text{and}$$

Phase Angle $\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$

The open loop gain $A_{OL}(f)$ dB is approximately constant from 0 Hz to the break frequency f_o.



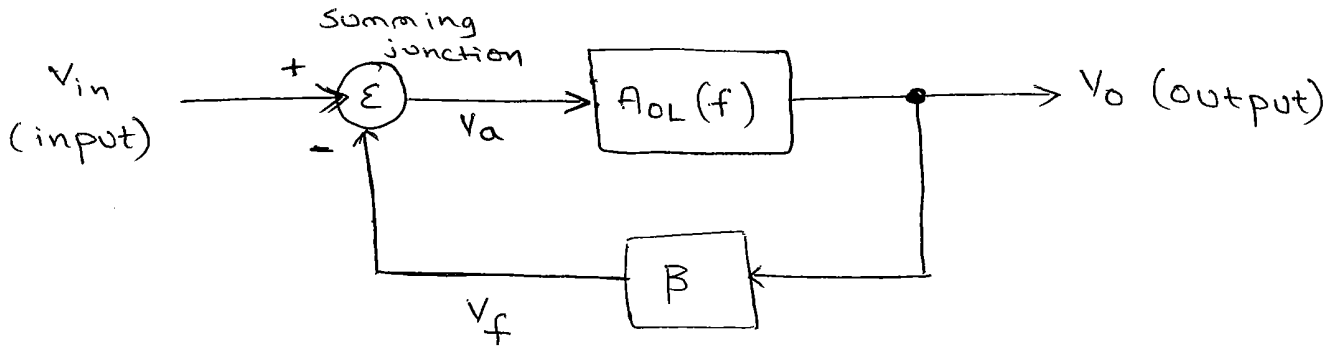


~~Open~~ closed loop frequency Response :

For an open loop op-Amp the band width is very small.

In order to increase the band width, a negative feedback must be used

A typical closed loop system (non inverting Amplifier)



$$A_{OL}(f) = \frac{V_o}{V_a} \quad \text{and} \quad \beta = \frac{V_f}{V_o}$$

$$V_a = V_{in} - V_f \quad \Rightarrow \quad V_{in} = V_a + V_f$$

$$A_{CL}(f) = \frac{V_o}{V_{in}} = \frac{V_o}{V_a + V_f}$$

$$A_{CL}(f) = \frac{V_o/V_o}{\frac{V_a}{V_o} + \frac{V_f}{V_o}} \Rightarrow \frac{1}{\frac{1}{A_{OL}(f)} + \beta}$$

$$A_{CL}(f) = \frac{A_{OL}(f)}{1 + A_{OL}(f)\,\beta}$$

System stability may be determined as follows.

Method 1 : Determine the phase Angle when the Magnitude of $A_{OL}(f)\,\beta$ is 0 dB or 1. If the phase angle is $> 180^\circ$, the system is stable. However for some systems the Magnitude may never be 0dB. in that Case method 2 must be used to determine the system stability.

Method 2 : Determine the Magnitude of $A_{OL}(f)\,\beta$ when the phase angle is -180°. If the Magnitude is negative decibels, then the system is stable. However some times the phase angle of a system may never reach -180°, under such conditions, Method 1 must be used to determine the system stability.

Slew Rate :

Slew Rate is defined as the maximum rate of change of output voltage with respect to time. a slew Rate is specified in units of $V/\mu s$.

The general purpose op-Amps such as 741 have a maximum slew rate of $0.5 V/\mu s$, which means that the output voltage can change at a maximum of $0.5V$ in $1\mu s$.

Causes for slew Rate :

The slew Rate is determined by a number of factors such as the amplifier gain, compensating capacitors and the change in polarity of output voltage It is also a function of temperature and the slew Rate generally reduces due to rise in temperature.

The capacitor within or outside the op-Amp is required to prevent oscillation and this capacitor restricts the response of op-Amp to a rapidly changing input signal. The rate at which the voltage across the capacitor V_c increases is given by

$$\frac{dV_c}{dt} = \frac{I}{C}$$

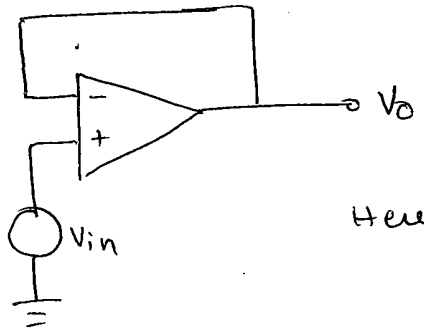
where I is the current furnished by the internal circuit. this means that the op-Amp must have either a higher current or a small Compensation capacitor.

For example IC 741 can provide 15 μA of maximum current to its internal 30PF capacitor. that is

$$\text{Slew Rate} = \left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\,\mu A}{30\,PF} = 0.5\,V/\mu s$$

Slew Rate Equation:

since the slew Rate is generally listed for a unity gain let us consider the voltage follower shown in figure below.



Here $V_o = V_{in}$

Let us assume that the input is a large amplitude and high frequency sine wave. The Equation for the sine wave is

$$V_{in} = V_p \sin \omega t$$

$$V_o = V_p \sin \omega t$$

The rate of change of the output is

$$\frac{dV_o}{dt} = V_p \omega \cos \omega t$$

and the maximum rate of change of output occurs when $\cos \omega t = 1$ that is

$$\left.\frac{dv_o}{dt}\right|_{max} = V_p \omega$$

$$\text{Slew Rate} = 2\pi f V_p$$

$$\text{Slew Rate} = \frac{2\pi f V_p}{10^6} \text{ V}/\mu\text{s}$$

The maximum frequency f_{max} at which an undistorted output voltage with a peak value V_p can be obtained is determined by

$$f_{max} = \frac{\text{Slew Rate} \times 10^6}{2\pi V_p}$$

The maximum peak sinusoidal output voltage $(V_p)_{max}$ that can be obtained at a frequency of f is given by

$$(V_p)_{max} = \frac{\text{Slew Rate} \times 10^6}{2\pi f}$$

Problem: The op-Amp 741 Connected as a unity gain inverting amplifier is applied with a input change of 10V. Determine the time taken for the output to change by 10V.

Solution: For op-Amp Slew Rate $= 0.5 \text{ V}/\mu\text{s}$

$$\text{Slew Rate} = \frac{\text{output voltage change}}{\text{Time}}$$

$$\text{Time} = \frac{10\text{V}}{0.5\text{ V}/\mu\text{s}} = 20\mu\text{s}.$$

problem: The slew Rate for 741 is $0.5 \text{ V}/\mu\text{s}$. What is the maximum undistorted sine wave that can be obtained for 12V peak.

$$f_{max} = \frac{\text{Slew Rate} \times 10^6}{2\pi V_m} = \frac{0.5 \times 10^6}{2\pi \times 12} = 6.63\,kHz.$$

Problem: The 741C is used as an inverting amplifier with a gain of 50. The sinusoidal input signal has a variable frequency and maximum frequency of the input Aplitude of 20mV peak. what is max at which the output will be undistorted? Assume that the amplifier is initially nulled.

Solution: $A = \frac{V_o}{V_{id}} \Rightarrow V_o = A V_{id} = 50 \times 20mV$

$$V_o = 1000 \times 10^{-3} V = 1 V (peak) = V_p$$

$$f_{max} = \frac{SR \times 10^6}{2\pi V_p} = \frac{0.5 \times 10^6}{2\pi \times 1} = 79.6\,kHz.$$

problem: An inverting amplifier using the 741C must have a flat response upto 40KHz. The gain of the amplifier is 10. what maximum peak to peak input signal can be applied with out distorting the output?

solution: slew Rate of 741 op-Amp $= 0.5\,V/\mu s$

$$SR = \frac{2\pi f V_p}{10^6}$$

$$(V_p)_{max} = \frac{SR \times 10^6}{2\pi f} = \frac{0.5 \times 10^6}{2\pi \times 40 \times 10^3} = 1.99\,V$$

$$V_p = 1.99\,V = V_o$$

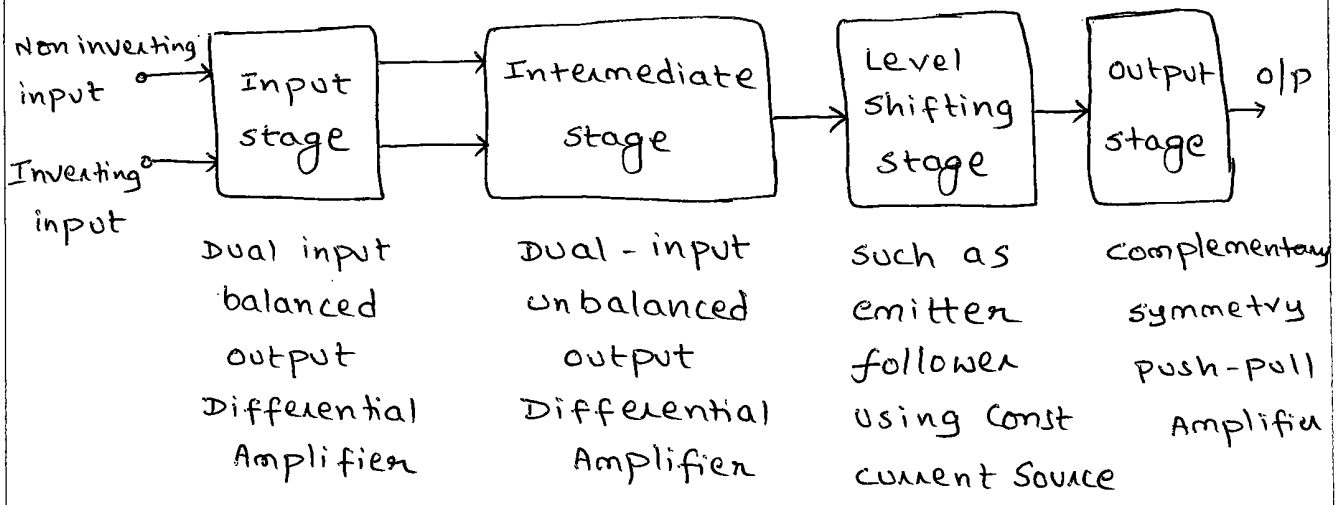
$$(V_o)_{peak} = 1.99V \Rightarrow (V_o)_{peak\ to\ peak} = 3.98V$$

$$A = \frac{(V_o)_{peak\ to\ peak}}{(V_{in})_{peak\ to\ peak}} \Rightarrow A = \frac{3.98}{(V_{in})_{peak\ to\ peak}}$$

$$(V_{in})_{peak\ to\ peak} = \frac{3.98}{10} = 0.398V.$$

Op-Amp Internal circuit

Op-Amps usually consists of four cascaded blocks. The block diagram of IC Op-Amp is shown in figure below.



Input stage:

The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals. It also requires low output impedance. All such requirements are achieved by using the dual input, balanced output differential amplifier as the input stage. The function of a differential amplifier is to amplify the difference between the two input signals. The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier

Intermediate stage:

The output of the input stage drives the next stage which is a intermediate stage. This is another differential amplifier with Dual input unbalanced output ie. single ended output. The overall gain requirement of the op-Amp is very high. The input stage alone cannot provide such a high gain. The main function of the Intermediate stage is to provide an additional voltage gain required. practically the intermediate stage is not a single amplifier but the chain of cascaded amplifiers called as multistage Amplifiers.

3) Level shifting stage:

All the stages are directly coupled to each other. As the op-Amp amplifies d.c signals also, the coupling capacitors are not used to cascade the stages. Hence the dc quiescent voltage level of previous stage gets applied as the input to the next stage. Hence stage by stage dc level increases well above ground ~~level~~ potential. Such a high d.c level may drive the transistors into saturation. This further may cause distortion in the output due to clipping. this may limit the

maximum a.c output voltage swing with out any distortion. Hence before the output stage, it is necessary to bring such a high dc voltage level to zero volts with respect to ground.

The level shifter stage brings the dc level down to ground potential, when no signal is applied at the input terminals. Then the signal is given to the last stage which is the output stage.

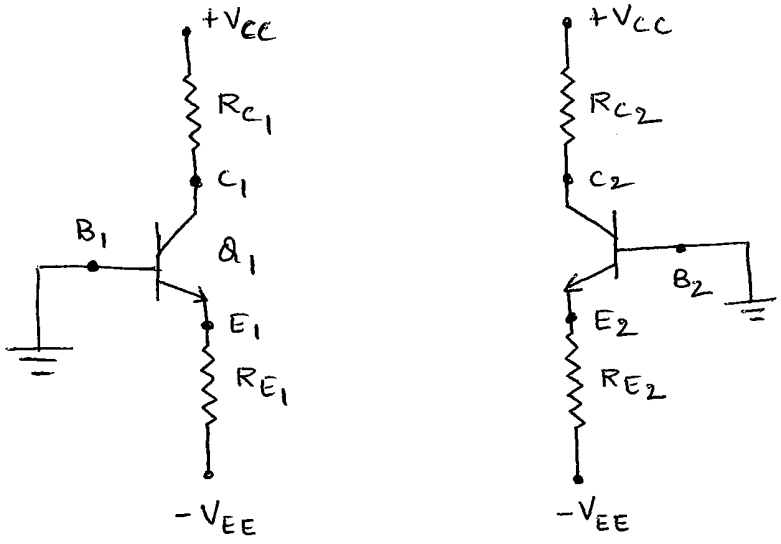
Output stage :

The basic requirements of an output stage are low output impedance, large ac output voltage swing and high current source and sinking capability.

The push pull complementary amplifier meets all these requirements and hence used as an output stage. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground. This stage raises the current supplying capability of the op-Amp.

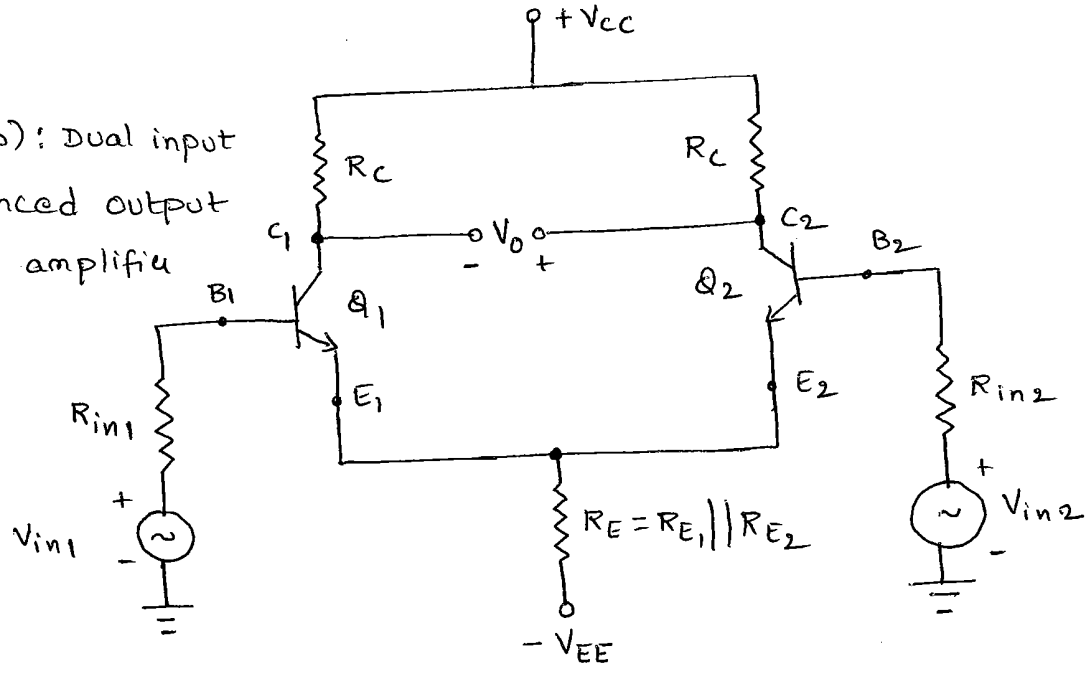
Differential Amplifier:

Let us consider the emitter biased circuit. Figure below shows two ~~emitter~~ identical emitter-biased circuits in that transistor Q_1 has the same characteristics as transistor Q_2. $R_{E_1} = R_{E_2}$, $R_{C_1} = R_{C_2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$ Here the supply voltages $+V_{CC}$ and $-V_{EE}$ are mear measured with respect to ground.



Fig(a): Two identical emitter-biased circuits

Fig(b): Dual input balanced output diff amplifier



the two circuits of fig(a) are reconnected to obtain a single circuit as shown in fig(b).

the differential amplifier of fig(b) amplifies the difference between two input signals V_{in1} and V_{in2}. the differential amplifier is also referred to as difference amplifier.

Differential Amplifier Circuit configurations :

the four differential amplifier configurations are

1. Dual input, balanced output differential amplifier
2. Dual input, unbalanced output differential amplifier
3. Single input, balanced output differential amplifier
4. Single input, unbalanced output differential amplifier.

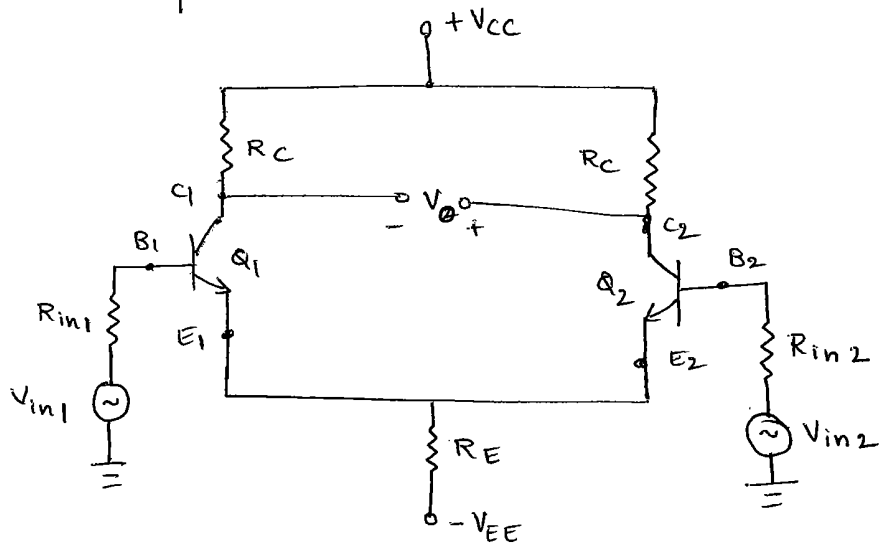
If we use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration.

If the output is measured between two collectors it is referred to as a balanced output, because both collectors are at the same dc potential with respect to ground.

If the output is measured at one of the collectors with respect to ground, the configuration is called an unbalanced output.

i) Dual input, Balanced output Differential Amplifier

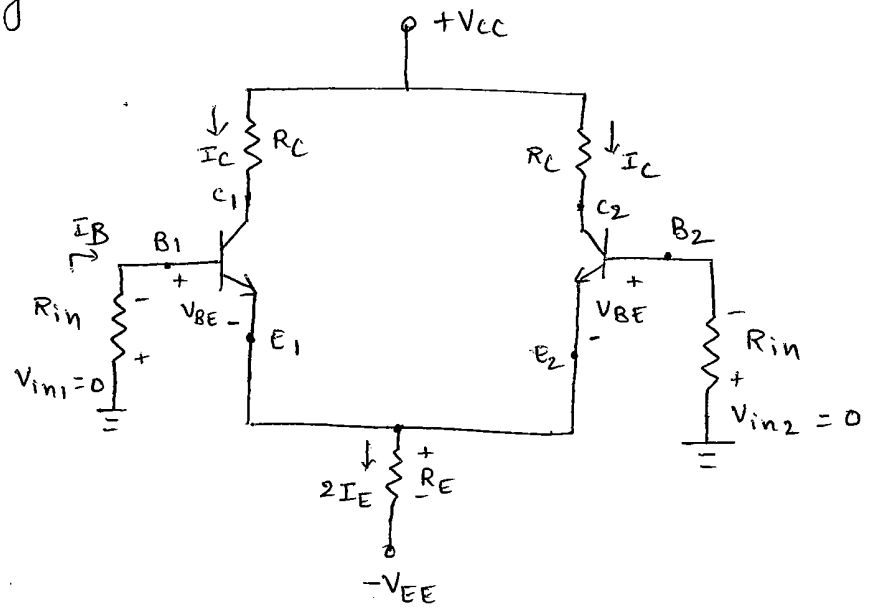
Figure below shows the dual input balanced output differential amplifier.



Fig(a): Dual input, balanced output differential Amplifier

Here the output V_o is measured between the two collectors C_1 and C_2 which are at the same dc potential. Because of the equal dc potential at the two collectors with respect to ground, the output is referred to as a balanced output.

Dc Analysis:



Fig(b): Dc Equivalent circuit of the dual input, balanced output differential amplifier.

To determine the operating values (I_{CQ} and V_{CEQ}) for the differential amplifier of fig(a), it is needed to obtain a dc Equivalent circuit. The dc equivalent circuit can be obtained simply by reducing the input signals V_{in1} and V_{in2} to zero. The dc Equivalent circuit is shown in figure (b).

Since both emitter-biased junctions of the differential amplifier are symmetrical, the operating point (V_{CEQ}, I_{CQ}), for only one section (Q_1) can be determined. these V_{CEQ} and I_{CQ} can then be used for transistor Q_2 also.

Applying KVL to the base emitter loop of the transistors Q_1

$$0 = R_{in} I_B + V_{BE} + 2 I_E R_E - V_{EE} \longrightarrow (1)$$

But $I_C = \beta I_B$ since $I_C \simeq I_E$

$$I_E = \beta_{dc} I_B \Rightarrow I_B = \frac{I_E}{\beta_{dc}} \longrightarrow (2)$$

From Eq (1) & (2) $I_E = \dfrac{V_{EE} - V_{BE}}{2R_E + \cdots}$

From Eq (1) & (2), $V_{EE} = V_{BE} + 2R_E \dfrac{I_E}{\beta_{dc}} + R_{in} \dfrac{I_E}{\beta_{dc}}$

$$V_{EE} = V_{BE} + I_E \left[2R_E + \frac{R_{in}}{\beta_{dc}} \right]$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \dfrac{R_{in}}{\beta_{dc}}} \longrightarrow (3)$$

Emitter current in transistors Q_1 and Q_2

Generally $\frac{R_{in}}{\beta_{dc}} << 2R_E$, therefore eq (3) can be written as

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \longrightarrow (4)$$

By selecting the proper value of R_E, the desired value of emitter current for a known value of $-V_{EE}$.

The voltage at the emitter of transistor Q_1 is approximately equal to $-V_{BE}$, if we assume that voltage drop across R_{in} to be negligibly small.

$$V_C = V_{CC} - I_C R_C$$

But $V_{CE} = V_C - V_E$

$$V_{CE} = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \longrightarrow (5)$$

Hence for both transistors, the I_{CQ} and V_{CEQ} by Equations (4) and (5) can be determined because the operating point $I_E = I_{CQ}$ and $V_{CE} = V_{CEQ}$.

AC analysis :

To perform ac analysis to derive the expression for the voltage gain Ad and the input resistance R_i of the differential amplifier shown in figure (a)

1. set the dc voltages $+V_{CC}$ and $-V_{EE}$ at zero
2. Substitute the small-signal T-equivalent models for the transistors.

Figure (c) shows the resulting ac equivalent circuit of the dual-input, balanced output differential amplifier

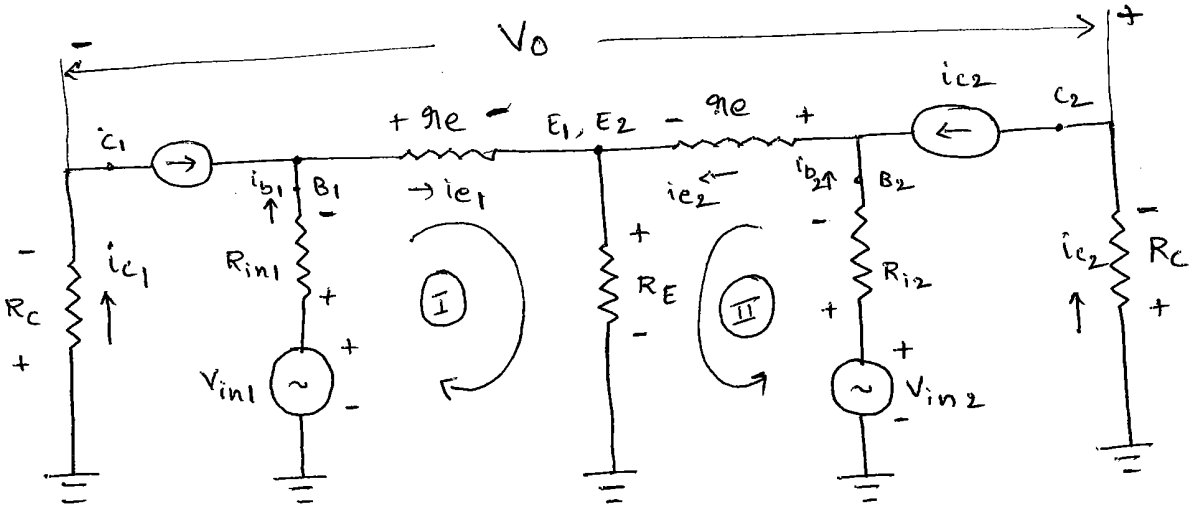


Fig C: Ac Equivalent ckt

writing KVL for loops I and II in figure (c)

$$V_{in1} = R_{in1} i_{b1} + i_{e1} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (1)$$

$$V_{in2} = i_{b2} R_{in2} + i_{e2} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (2)$$

$$i_{b1} = \frac{i_{e1}}{\beta_{ac}} \qquad i_{b2} = \frac{i_{e2}}{\beta_{ac}}$$

Generally $\frac{R_{in1}}{\beta_{ac}}$ and $\frac{R_{in2}}{\beta_{ac}}$ values are very small. therefore we shall neglect them

$$V_{in1} = \frac{R_{in1}}{\beta_{ac}} i_{e1} + i_{e1} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (3)$$

$$V_{in2} = \frac{R_{in2}}{\beta_{ac}} i_{e2} + i_{e2} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (4)$$

$$\therefore V_{in1} = (r_e + R_E) i_{e1} + R_E i_{e2} \longrightarrow (5)$$

$$V_{in2} = R_E i_{e1} + (r_e + R_e) i_{e2} \longrightarrow (6)$$

Equations (5) and (6) can be solved simutaneously for ie_1 and ie_2 by using Cramer's rule.

$$ie_1 = \frac{\Delta_1}{\Delta} = \frac{\begin{vmatrix} V_{in1} & RE \\ V_{in2} & r_e + RE \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$ie_1 = \frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - (R_E)^2} \longrightarrow (7)$$

$$ie_2 = \frac{\Delta_2}{\Delta} = \frac{\begin{vmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$ie_2 = \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - (R_E)^2} \longrightarrow (8)$$

The output voltage $V_o = V_{c_2} - V_{c_1}$

$$V_o = -ic_2 R_C - (-ic_1 R_C)$$

$$V_o = R_C (ic_1 - ic_2)$$

$$V_o = R_C (ie_1 - ie_2) \longrightarrow (9)$$

Substituting the current relations ie_1 and ie_2 in Eq (9) we get

$$V_o = R_C \left[\frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2} - \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$V_o = \frac{R_c}{r_e}(V_{in1} - V_{in2})$$

Let $V_d = V_{in1} - V_{in2}$, then

$$V_o = \frac{R_c}{r_e} V_d \quad \Rightarrow \quad A_d = \frac{V_o}{V_d} = \frac{R_c}{r_e} \longrightarrow (10)$$

The voltage gain equation of the differential amplifier is independent of R_E.

2. Differential input Resistance :

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminals with the other terminal grounded.

$$R_{i1} = \left| \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=0}$$

$$R_{i1} = \left| \frac{V_{in1}}{I_{e1}/\beta_{ac}} \right| = \frac{\beta_{ac} V_{in1}}{\dfrac{(r_e + R_E) V_{in1} - R_E(0)}{(r_e + R_E)^2 - R_E^2}}$$

$$R_{i1} = \frac{\beta_{ac} (r_e^2 + 2 r_e R_E)}{(r_e + R_E)}$$

$$R_{i1} = \frac{\beta_{ac} \; r_e (r_e + 2R_E)}{(r_e + R_E)}$$

$R_E \gg r_e$ which implies that $r_e + 2R_E \simeq 2R_E$

$r_e + R_E \simeq R_E$

$$R_{i1} = \frac{\beta_{ac} \; r_e \; 2R_E}{R_E}$$

$$R_{i1} = 2\beta_{ac} r_e$$

Similarly $R_{i2} = 2\beta_{ac} r_e$.

Output Resistance:

Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground.

$$R_{o1} = R_{o2} = R_C.$$

Inverting and Non inverting Inputs:

In the differential amplifier circuit the input voltage V_{in1} is called the non inverting input because a positive voltage V_{in1} acting alone produces a positive output voltage.

$$V_o = \frac{R_C}{r_e}(V_{in1} - 0) = \frac{R_C}{r_e} V_{in1}$$

Similarly the positive voltage V_{in2} acting alone produces a negative output voltage, hence V_{in2} is called inverting input.

$$V_o = \frac{R_C}{r_e}(0 - V_{in2}) = -\frac{R_C}{r_e} V_{in2}.$$

Common mode Rejection Ratio:

An important characteristic of the dual input balanced output differential amplifier is its ability to supress undesired disturbances that might be amplified along with the desired signal.

when the matched pair of transistors is used in the differential amplifier, the unwanted signals would appear as common to both input bases, and the net output would be theoretically zero.

The practical effectiveness of rejecting the common signal depends on the degree of matching between the two common-emitter stages forming the differential amplifier.

In other words, the more closely equal are the currents in the input transistors Q_1 and Q_2 the better is the common mode signal rejection.

When the same voltage is applied to both input terminals of a differential amplifier, the differential amplifier is said to operate in the common mode configuration.

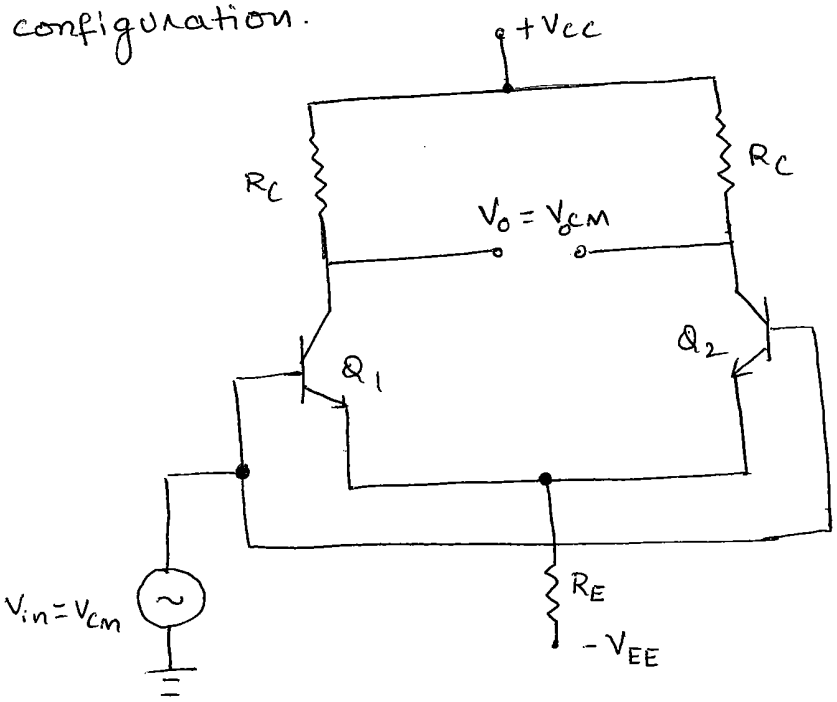


Figure: Differential amplifier in common mode configuration.

The ability of a differential amplifier to reject a common mode signal is expressed by its "Common mode

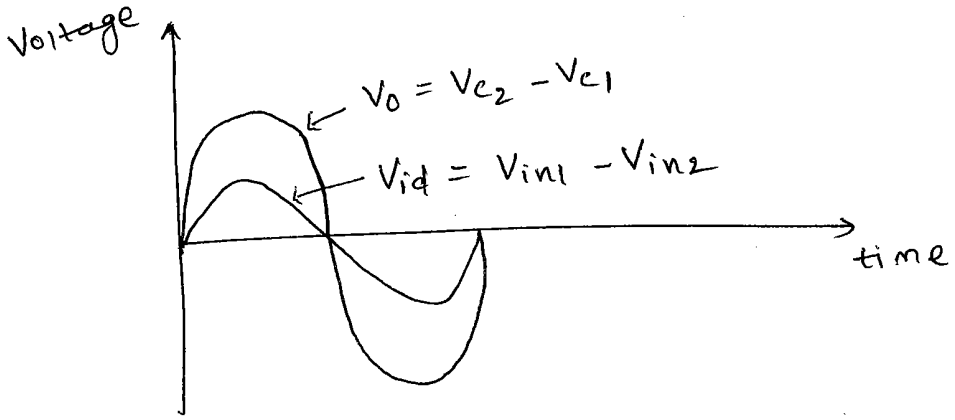
Rejection Ratio" (CMRR). It is the ratio of differential gain A_{DM} to the common mode gain A_{CM}

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

the common mode voltage gain A_{CM} can be as follows. The known voltage A_{CM} to both input terminals of the differential amplifier is applied as shown in figure above. Here $A_{CM} = \frac{V_{OCM}}{V_{CM}}$

Ideally A_{CM} to be zero that is $V_{OCM} = 0$ V. In other words CMRR is ideally infinity. Thus it is advantageous to use a differential amplifier with higher CMRR since this amplifier is better able to reject common mode signals.

Input output wave forms



Dual input unbalanced output Differential Amplifier :

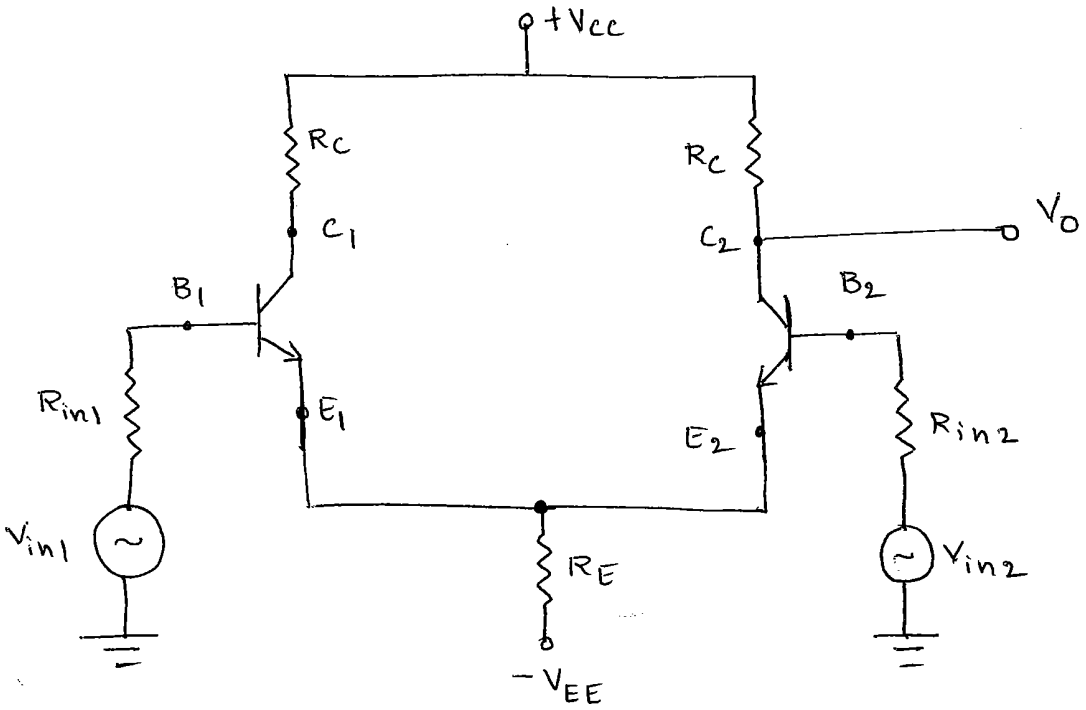
In this configuration two input signals are used. however the output is measured at only one of the two collectors with respect to ground. The output is refered to as an unbalanced output.

Let us assume that the output is measured at the collector of transistor Q_2 with respect to ground.

DC Analysis :

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}}$$

$$V_{CE} = V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$



Fig(a): Dual input unbalanced output Differential Amplifier

AC Analysis : Fig below shows the ac equivalent circuit of the dual input, unbalanced output differential

amplifier with small signal T-equivalent models substituted for the transistors.

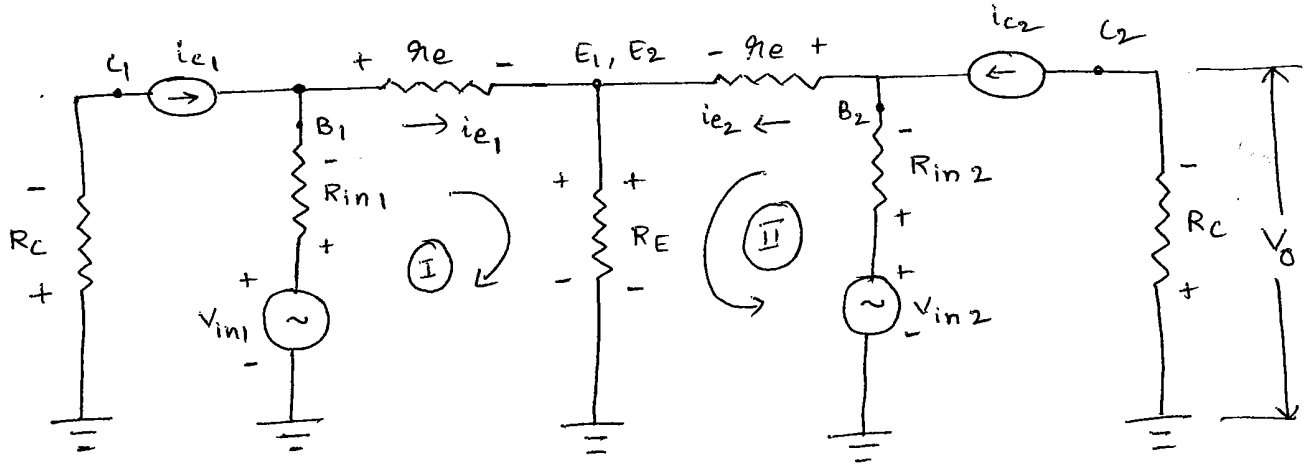


Fig (b) ; AC Equivalent circuit.

Voltage gain : writing KVL for loops (I) and II

$$V_{in1} = R_{in1} i_{b1} + r_e i_{e1} + R_E (i_{e1} + i_{e2})$$

$$V_{in2} = R_{in2} i_{b2} + r_e i_{e2} + R_E (i_{e1} + i_{e2})$$

$$i_{e1} = \frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2}$$

$$i_{e2} = \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = V_{c2} = V_{cc} - i_{c2} R_C = -R_C i_{c2} = -R_C i_{e2}$$

$$V_o = -R_C \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = R_C \frac{R_E V_{in1} - (r_e + R_E) V_{in2}}{r_e (r_e + 2R_E)}$$

Generally $R_E >> r_e$, hence $r_e + R_E \simeq R_E$, $r_e + 2R_E \simeq 2R_E$

$$\therefore \quad V_o = R_c \frac{R_E V_{in1} - R_E V_{in2}}{2 r_e R_E}$$

$$V_o = \frac{R_c}{2 r_e} (V_{in1} - V_{in2})$$

$$A_d = \frac{V_o}{V_d} = \frac{R_c}{2 r_e}$$

Thus the voltage gain of the dual input unbalanced output differential amplifier is half the gain of the dual input balanced output differential amplifier.

Differential input resistance :

$$R_{i1} = R_{i2} = 2 \beta_{ac} r_e$$

Differential output resistance

$$R_{o1} = R_{o2} = R_c$$

Level Translator (Level shifting stage) :

Because of the direct coupling, the dc level at the emitters rises from stage to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

The voltage at the output terminal of the second stage is well above ground (0V). This dc level is undesirable because it tends to limit the peak to peak output voltage swing without distortion and

also contributes to the error in the dc output signal.

Therefore a final stage should be included to shift the output dc level at the second stage down to about zero volts to ground. such a stage is referred to as a level translator or shifter. thus in the cascaded differential amplifier, to shift the output dc level down to zero volts, the final stage must be followed by a level translator circuit.

A simplest level translator circuit is an emitter follower with a voltage divider circuit. is shown in figure below.

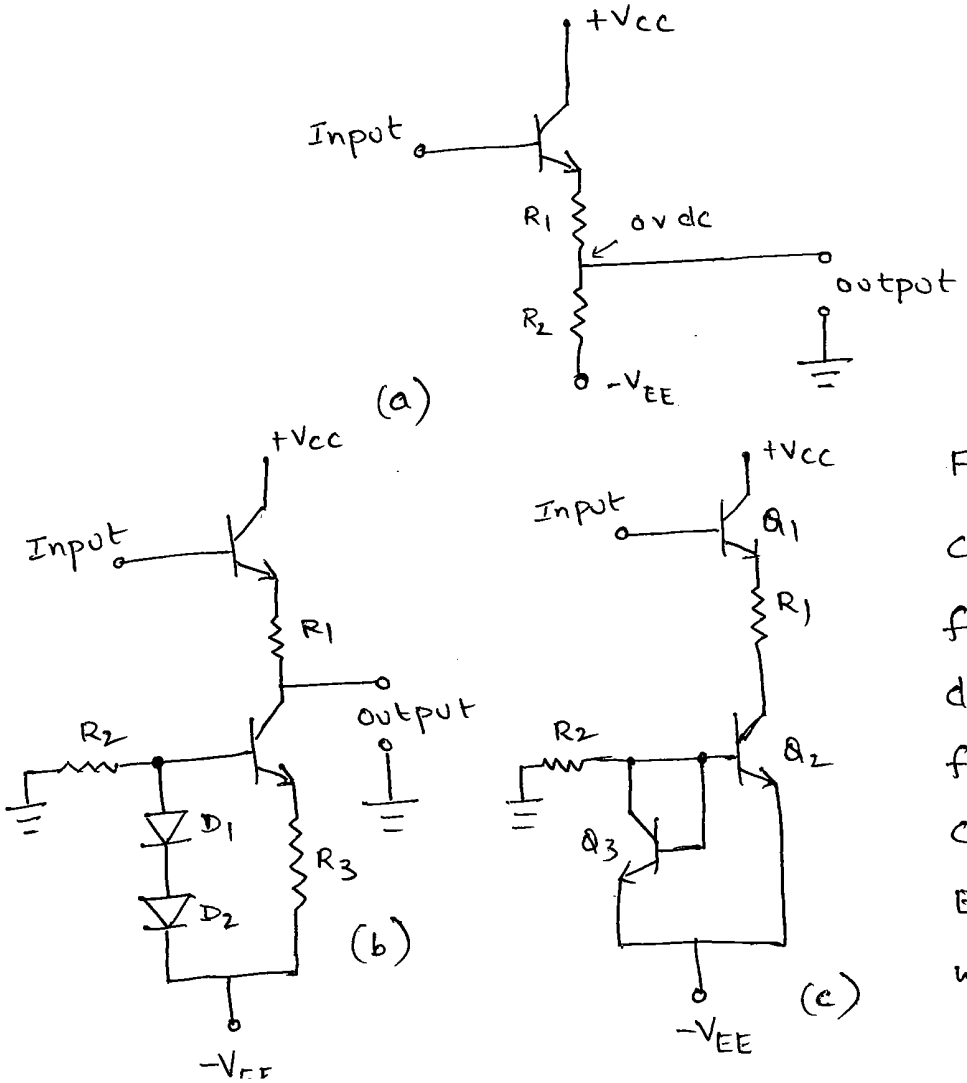
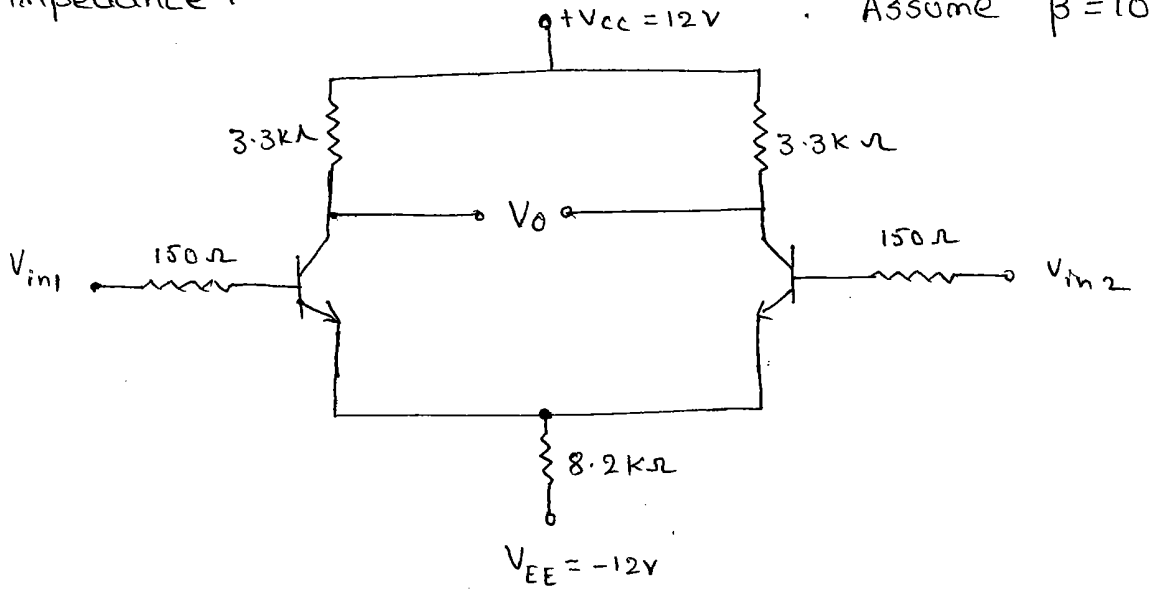


Fig: Level translator circuits (a) Emitter follower with voltage divider (b) Emitter follower with constant current bias (c) Emitter follower with current mirror.

Problem: For the differential amplifier shown in figure below. calculate

i) operating point 2) voltage gain 3) Input and output impedance. Assume $\beta = 100$



Solution: $R_C = 3.3k\Omega$, $R_{in} = 150\Omega$, $R_E = 8.2k\Omega$

$V_{cc} = 12V = -V_{EE}$, $\beta = 100$

i) $$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta}} = \frac{12 - 0.7}{\frac{150}{100} + 2 * 8.2 \times 10^3} = 0.688\,mA.$$

$$I_{CQ} = I_E = 0.688\,mA$$

$$V_{CEQ} = V_{cc} + V_{BE} - I_{CQ} R_C = 12 + 0.7 - \left(0.688 \times 10^{-3} \times 3.3 \times 10^3\right)$$

$$V_{CEQ} = 10.42V$$

(ii) $$r_e = \frac{25\,mV}{I_E} =$$

$$\therefore A_d = \frac{R_C}{r_e}$$

As the configuration is dual input balanced output

iii) $R_i = 2 h_{ie} \beta = 2x$

(iv) $R_O = R_C = 3.3 K\Omega$.

Problem: If the base currents for the emitter coupled transistors of a differential amplifier are 18μA and 22μA. Determine

i) Input bias current (ii) Input offset current for an op-Amp.

Solution: $I_{b_1}^{+} = 18\mu A$, $I_{b_2}^{-} = 22\mu A$

(i) Input bias current $I_b = \frac{I_{b_1}^{+} + I_{b_2}^{-}}{2} = \frac{18+22}{2} = 20\mu A$

(ii) Input offset current

$$I_{ios} = |I_{b_1}^{+} - I_{b_2}^{-}| = |18 - 22| = 4\mu A.$$

Problem:

An op-Amp operates as a unity gain buffer with 3V (peak to peak) square wave input. If op-Amp is ideal with slew rate 0.5 V/μs. Find the maximum frequency of operation.

Solution: $V_{p-p} = 3V \Rightarrow V_p = \frac{V_{p-p}}{2} = \frac{3}{2} = 1.5V$

$$f_{max} = \frac{\text{slew rate} \times 10^6}{2\pi V_p} = \frac{0.5 \times 10^6}{2\pi \times 1.5} = 53.05 KHz$$

Problem: A square wave of peak to peak amplitude of 750 mV has to be amplified to a peak to peak amplitude of 3.8V, with a rise time of 4.5 μsec or less. Can IC 741 op-Amp be used?

Solution: $SR = \frac{\Delta V}{\Delta t}$, IC 741 has $SR = 0.5\ V/\mu sec$

Now Rise time is the time required by the output to rise from 10% to 90% of its final value

$$\Delta V = (0.9 - 0.1)\ 3.8\ V = 3.04\ V.$$

$$\Delta t = 4.5\ \mu sec$$

$$SR = \frac{\Delta V}{\Delta t} = \frac{3.04V}{4.5\ \mu} = 0.675\ V/\mu sec.$$

The slew Rate of IC 741 is 0.5 V/μsec which is too low compared to what is required. Hence IC 741 op-Amp cannot be used.

Problem: In response to a square wave input, the output of an op-Amp changed from -3V to +3V over a time interval of 0.25 V/μs. Determine the slew Rate of the op-Amp.

Solution: change in output voltage = -3V to +3V

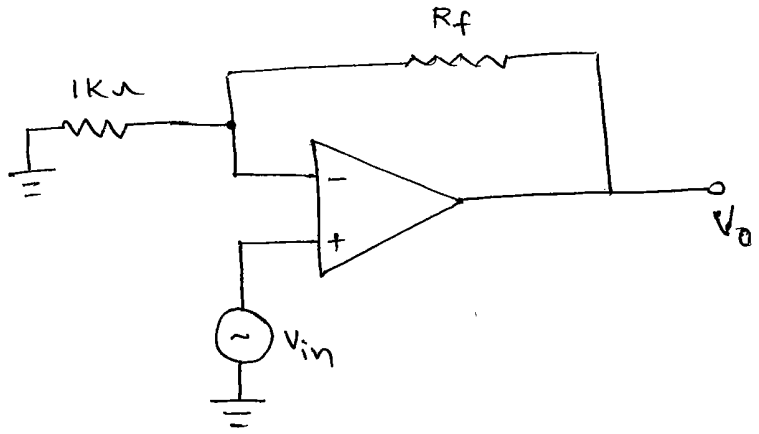
$$dV_0 = 3 - (-3) = 6V$$

$$dt = 0.25\ V/\mu s.$$

$$\text{slew Rate} = \frac{dV_0}{dt} = \frac{6}{0.25\ \mu s} = 24\ V/\mu s.$$

problem: For the op-Amp configuration shown in figure below. the gain required is 61. Determine the appro-priate value of feedback resistor R_f.

solution:



solution: $$\text{Gain} = 1 + \frac{R_f}{R_1} \Rightarrow 61 - 1 = \frac{R_f}{R_1}$$

$$R_f = 60\, R_1 = 60 \times 1K\Omega = 60K\Omega.$$

problem: For an op-Amp having a slew rate of $3\ V/\mu s$. what is the maximum closed loop voltage gain that can be used when the input signal varies by $0.4\ V$ in $12\ \mu sec$?

Solution: $$V_o = A\, V_i$$

$$\frac{dV_o}{dt} = A\,\frac{dV_i}{dt}$$

$$\text{Slew rate} = A\,\frac{dV_i}{dt} \Rightarrow A = \frac{SR}{\frac{dV_i}{dt}}$$

$$\Rightarrow A = \frac{\frac{3}{10^{-6}}}{\frac{0.4}{12 \times 10^{-6}}} = 90.$$

Problem: The common mode input to a certain differential amplifier, having differential gain of 125 is $4 \sin 200\pi t$ V. Determine the common mode output if CMRR is 60 dB.

Solution: The CMRR in dB is

$$60 = 20 \log \left| \frac{A_d}{A_c} \right|$$

$$\frac{A_d}{A_c} = 1000 \quad \Rightarrow \quad A_c = \frac{A_d}{1000} = \frac{125}{1000} = 0.125$$

Hence the common mode output is $= A_c V_c$

$$= 0.125 \left(4 \sin 200\pi t \right) = 0.5 \sin(200\pi t) \text{ V}$$

Problem: How fast can the output of an op-Amp change by 10V if its slew Rate is $1 \text{V}/\mu\text{s}$.

Solution:

$$SR = 1 \text{V}/\mu\text{s}$$

$$SR = \frac{\Delta V_o}{\Delta t} \quad \Rightarrow \quad \Delta t = \frac{\Delta V_o}{SR}$$

$$\Delta t = \frac{10 \text{V}}{1 \text{V}/\mu\text{s}} = 10 \, \mu\text{s}$$

Thus 10 μsec will be required by an op-Amp to change output by 10V.

D/A and A/D Converts

Introduction: most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convinient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital and digital to analog conversion.

D to A Converters

Basic DAC techniques:

The schematic of a DAC is shown in fig. The input is a binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

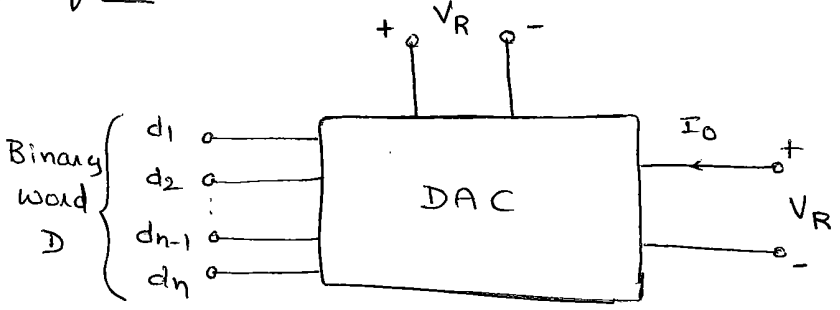


Fig: Schematic of DAC

$$V_0 = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \text{----} + d_n 2^{-n} \right) \longrightarrow (1)$$

where V_0 = output voltage

V_{FS} = Full scale output voltage

K = scaling factor usually adjusted to unity

$d_1, d_2 \text{ ---- } d_n$ = n-bit binary fractional word with the decimal point located at the left.

d_1 = MSB with a weight of $V_{FS}/2$

d_n = LSB with a weight of $V_{FS}/2^n$.

1) Weighted Resistor DAC:

One of the simplest circuits shown in figure below uses a summing Amplifier with a binary weighted resistor network.

It has n electronic switches $d_1, d_2 \cdots d_n$ controlled by binary input word. these switches are single pole double throw type. (SPDT).

If the binary input to a particular switch is 1, it connects a reference voltage $(-V_R)$. And if the input bit is 0, the switch connects the resistor to the ground. from the figure, the output current I_0 for an ideal op-Amp can be written as

$$I_0 = I_1 + I_2 + I_3 + \text{---} + I_n$$

$$I_0 = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \text{---} + \frac{V_R}{2^n R} d_n$$

$$V_o = \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \text{------} + d_n 2^{-n}\right)$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \text{---} + d_n 2^{-n}\right) \rightarrow (2)$$

comparing Eq (2) with Eq (1), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

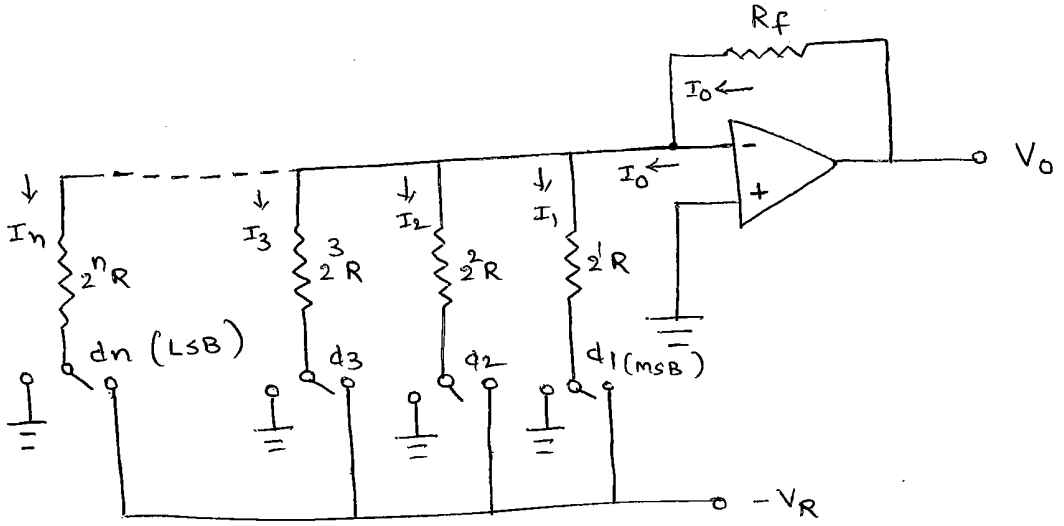
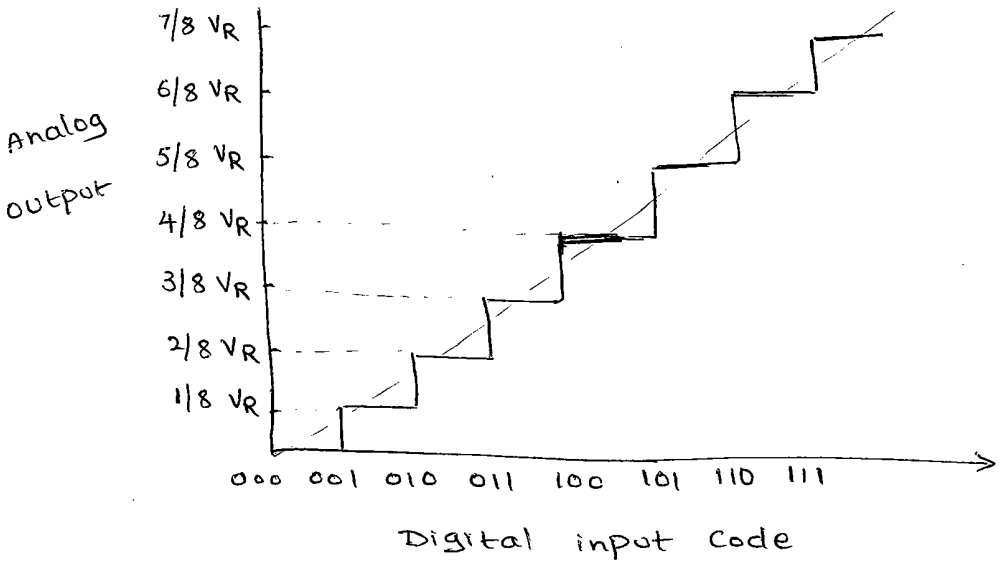


Fig (a): A simple weighted resistor DAC



Fig(b): Transfer characteristics of a 3-bit DAC

If $D = 100$, $V_o = V_R \frac{R_f}{R}\left(1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3}\right)$

$$V_o = \frac{V_R}{2} = \frac{4V_R}{8}$$

the circuit shown in above figure uses a negative reference voltage. the analog output voltage is therefore positive stair case as shown in figure(b). for a 3-bit weighted resistor DAC. It may be noted that

1) Although the op-Amp is connected in inverting mode, it can also be connected in non-inverting mode.
2) The op-Amp is simply working as a current to voltage converter.
3) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5V, and the output will be negative.

2) R-2R Ladder DAC

wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10 KΩ.

For simplicity, consider a 3-bit DAC as shown in figure below, where the switch position $d_1 d_2 d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of fig(b) and finally to fig(c). Then voltage at node c can be easily calculated by the set procedure of network analysis as

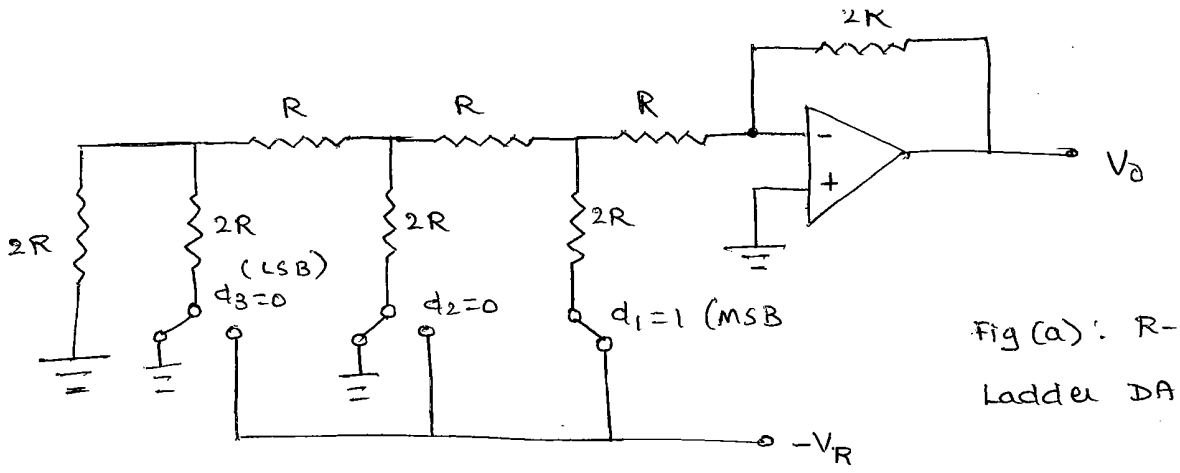
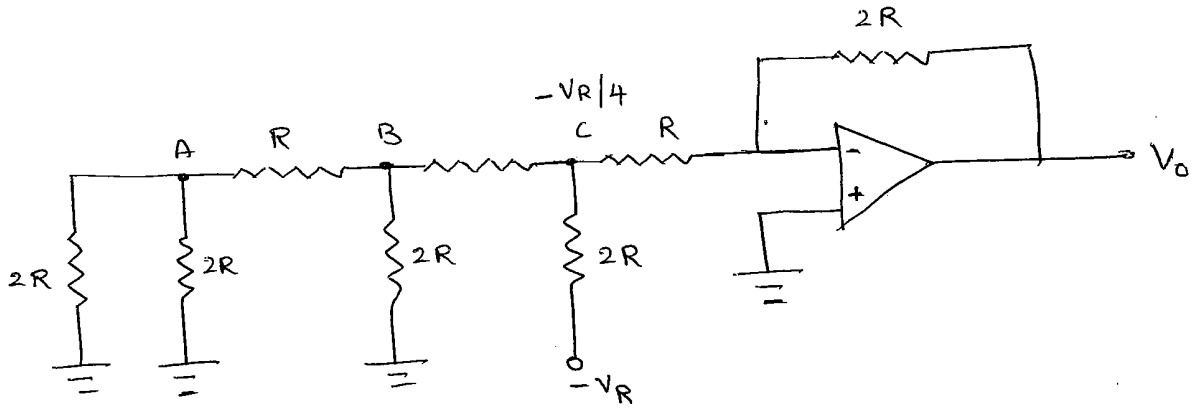


Fig (a): R-2R Ladder DAC



Fig(b): Equivalent circuit of fig(a)

$$V_C = \frac{-V_R\left(\frac{2}{3}R\right)}{2R + \frac{2}{3}R} = -\frac{V_R}{4}$$

the output voltage

$$V_0 = -\frac{2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

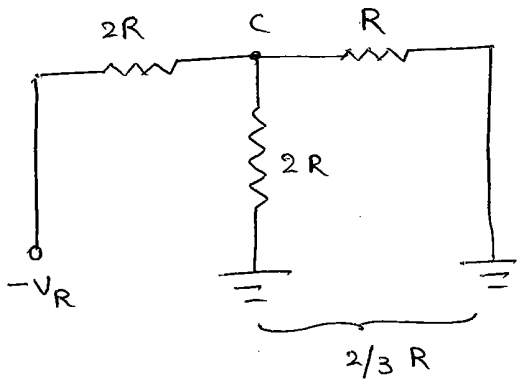


Fig c: Equivalent circuit of fig(b)

Similarly For binary word 001

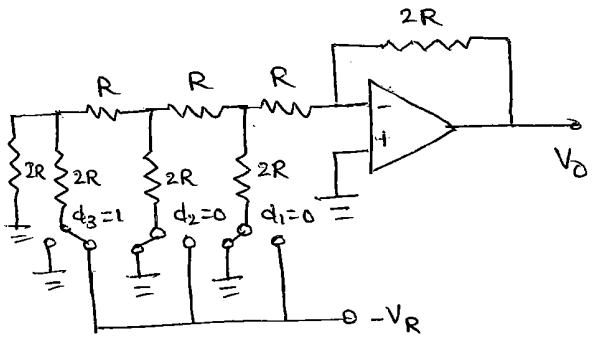
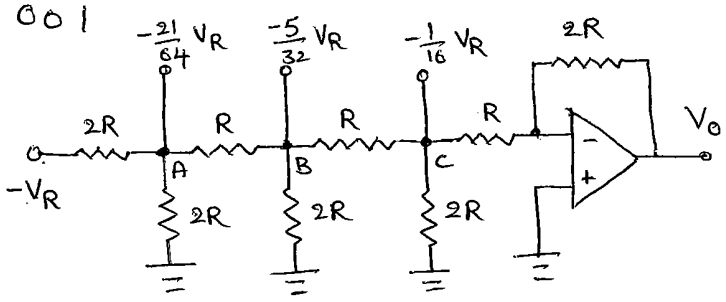


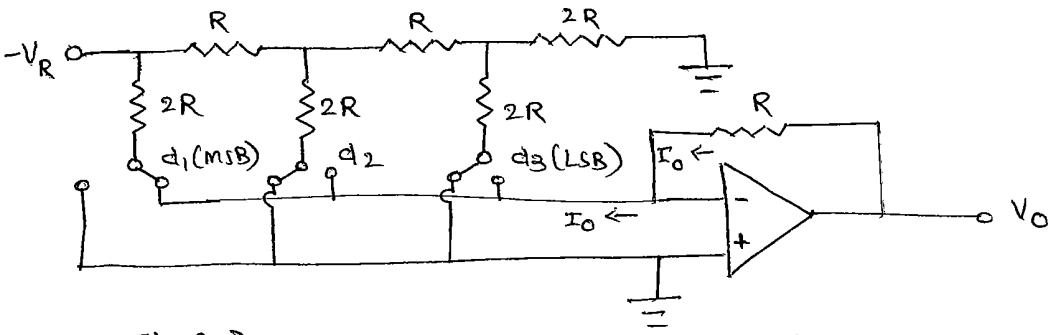
Fig: R-2R ladder DAC for switch position 001



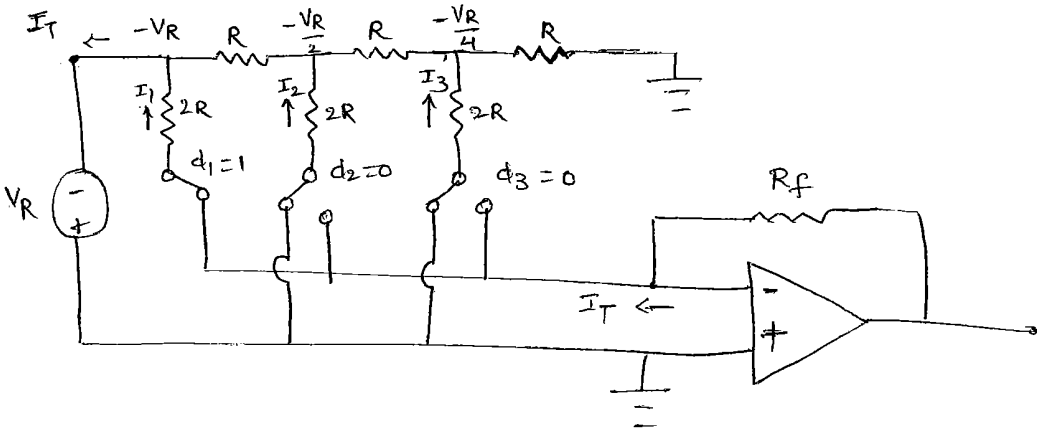
Fig(d): Equivalent circuit

$$V_0 = \left(-\frac{2R}{R}\right)\left(\frac{-V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

3) Inverted R-2R ladder DAC :



Fig(a) : Inverted R-2R Ladder DAC.



$$I_1 = \frac{V_R}{2R} \qquad I_2 = \frac{V_R}{2}\Big/2R = \frac{V_R}{4R} \qquad I_3 = \frac{V_R}{4}\Big/2R = \frac{V_R}{8R}$$

$$I_T = I_1 + I_2 + I_3$$

$$I_T = d_1\frac{V_R}{2R} + d_2\frac{V_R}{4R} + \frac{V_R}{8R}d_3 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

$$I_T = \frac{V_0 - 0}{R_f} \Rightarrow V_0 = I_T R_f$$

$$V_0 = V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

For 100 $\qquad V_0 = \frac{V_R}{2} \quad \left[\because R_f = R\right]$

In general

$$V_0 = V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}\right]$$

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. more power dissipation causes heating, which inturn creates non-linearity in DAC. This is a serious problem and can be avoided completely in Inverted ladder type DAC.

A 3-bit Inverted ladder type DAC is shown in figure, where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-Amp which is also at Virtual ground. since both the terminals of switches di are at ground potential, current flowing in the resistances is constant and independent of switch position.

Problem 1:

The basic step of a 9-bit DAC is 10.3mv. If 000000000 represents 0v, what output is produced if the input is 101101111?

Solution: The output voltage for input 101101111 is

$$= 10.3mv\left(1\times2^8 + 0\times2^7 + 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0\right)$$

$$= 3.78V.$$

Problem 2: calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10V range.

Solution: $LSB = \frac{10\,V}{2^8} = 39\,mV$

$MSB = \frac{10}{2} = 5\,V$

Full scale output = Full scale Voltage − 1 LSB

= 10 V − 39 mV = 9.961 V

Problem 3: what output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

i) 10 (for a 2-bit DAC)

ii) 0110 (for a 4-bit DAC)

iii) 10111100 (for a 8-bit DAC)

Solution: i) $V_0 = 10\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5\,V$

ii) $V_0 = 10\left(0 \times \frac{1}{2} + 1 \times \frac{1}{4} + 1 \times \frac{1}{8} + 0 \times \frac{1}{16}\right) = 3.75\,V$

iii) $V_0 = 10\left(1 \times \frac{1}{2} + 0 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 1 \times \frac{1}{2^4} + 1 \times \frac{1}{2^5} + 1 \times \frac{1}{2^6} + 0 \times \frac{1}{2^7} + 0 \times \frac{1}{2^8}\right) = 7.34\,V$

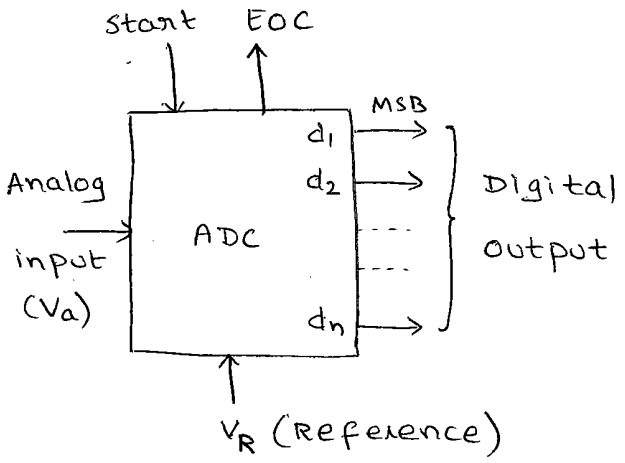
A-D Converters

The block schematic of ADC is shown in figure below It accepts an analog input voltage V_a and produces an output binary word $d_1, d_2 \cdots d_n$ of functional value D.

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}$$

where $d_1 \rightarrow$ MSB

d_n — LSB



An ADC usually has two additional control lines.

1. Start: used to tell the ADC when to start the conversion
2. End of Conversion (EOC): used to announce when the conversion is complete.

Depending upon the type of application, ADC's are designed for microprocessor interfacing or to directly drive LCD or LED displays.

ADC's are classified broadly in to two groups according to their conversion technique.

1. Direct type ADC's compare a given analog signal with the internally generated equivalent signal. This group includes
   1. Flash (comparator) type converter
   2. Counter type converter
   3. Tracking or servo Converter
   4. Successive approximation type converter.
2. Integrating type ADC's perform conversion in an indirect manner by first changing the analog input signal

to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are

i) charge balancing ADC

ii) Dual slope ADC

The most commonly used ADC's are successive approximation and the integrator type. The successive approximation ADC's are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash type is expensive for high degree of accuracy.

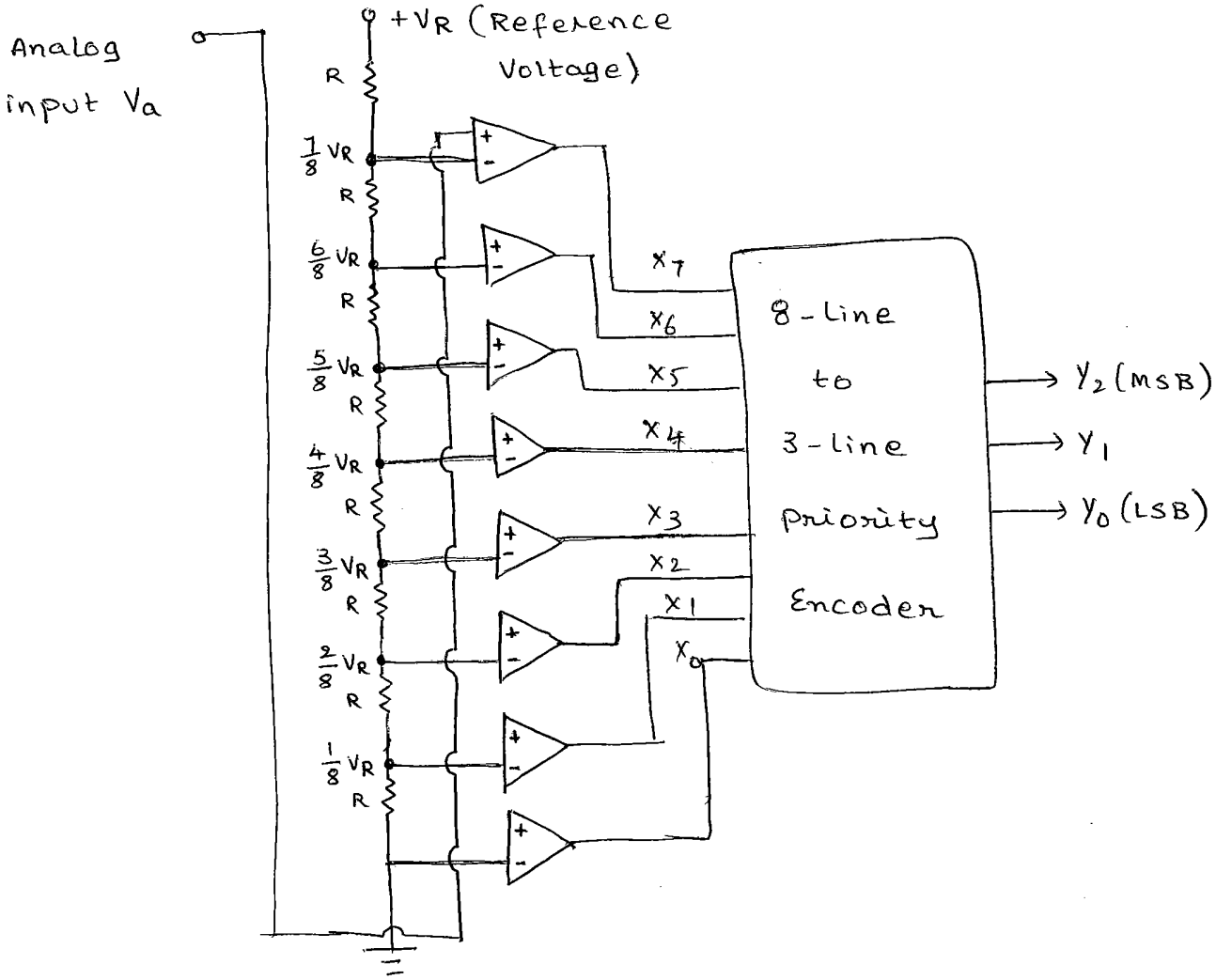
The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

Direct type ADC's:

1) Flash (Parallel Comparator) A/D converter:

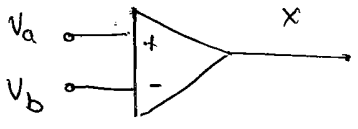
This is the simplest possible A/D Converter It is the fastest and most expensive technique. Figure below shows a 3-bit A/D converter. The circuit consists of resistor divider network, 8 OP-Amp comparators and a 8-line to 3 line Encoder. The comparator and its truth table is shown in figure below. ~~At~~ In fig(a) At each node of the resistive divider

a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage Va with each of the node voltages. The truth table of the flash type A/D converter is shown below.



Fig(a): Basic circuit of a Flash type A/D Converter

Voltage input	Logic output X
$V_a > V_b$	X = 1
$V_a < V_b$	X = 0
$V_a = V_b$	Previous Value



Fig(b): Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $2V_R/8$	0	0	0	0	0	0	1	1	0	0	1
$2V_R/8$ to $3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8$ to $4V_R/8$	0	0	0	0	1	1	1	1	0	1	1
$4V_R/8$ to $5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8$ to $6V_R/8$	0	0	1	1	1	1	1	1	1	0	1
$6V_R/8$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig (c): Truth table for a Flash type A/D Converter.

The circuit has the advantage of high speed as the conversion takes place simultaneously rather than sequentially. Typical conversion time 100ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder, Conversion delays of the order of 20ns can be obtained.

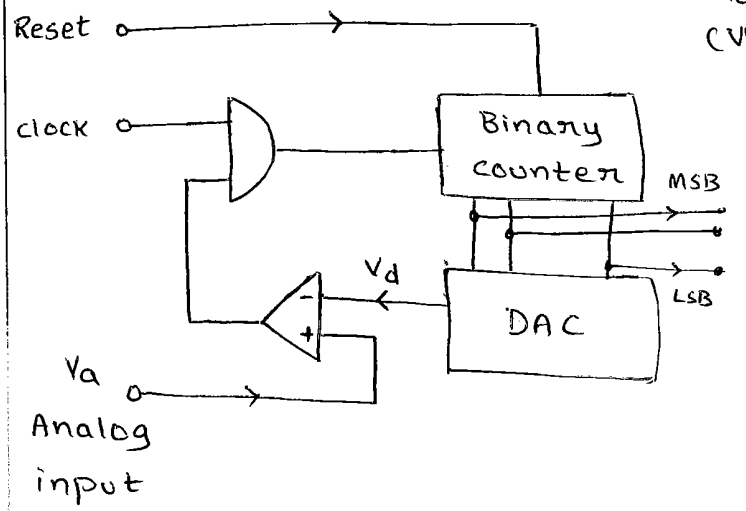
This type of ADC has the disadvantage that the number of comparators required doubles for each added bit. For Example n-bit ADC require 2^n comparators.

2) Counter type A/D Converter:

The D/A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes with in $\pm \frac{1}{2}$ LSB to the analog

input V_a which is to be converted to binary digital form.

A 3-bit counting ADC based upon the above principle is shown in figure below.



Fig(a): A Counter type A/D Converter

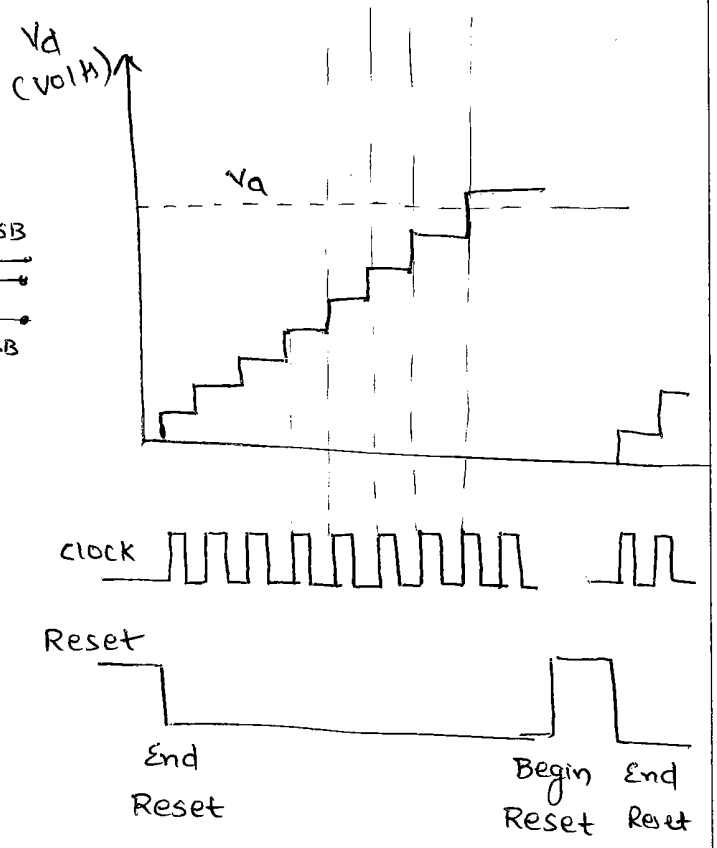


Fig (b): D/A output stair case waveform.

The counter is reset to zero count by the reset pulse. upon the release of reset, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the binary counter. Voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of the D/A converter whose output is the stair case shown in fig (b).

The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.

when $V_a < V_d$, the output of the Comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a.

For a new value of analog input V_a, a second reset pulse is applied to clear the counter. upon the end of the reset, the counting begins again as shown in fig(b). The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.

3) Successive Approximation converter:

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. ~~An~~

An Eight bit converter would require 8 clock pulses to obtain a digital output.

Fig (a) below shows an Eight bit Converter.

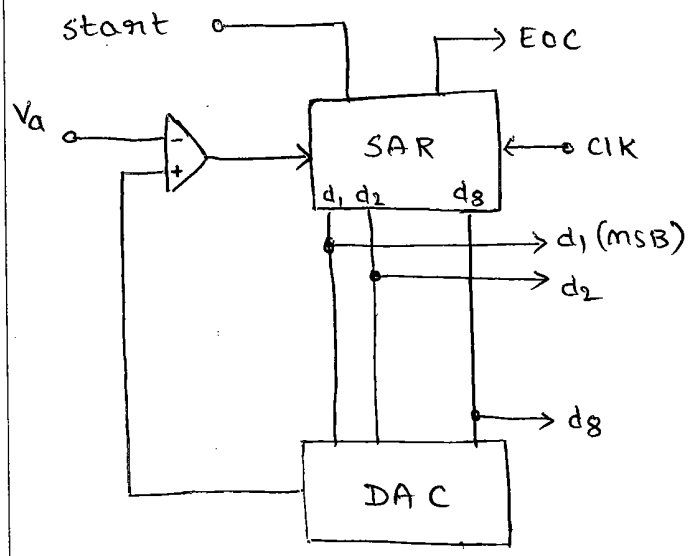


Fig: Functional diagram of the successive Approximation ADC

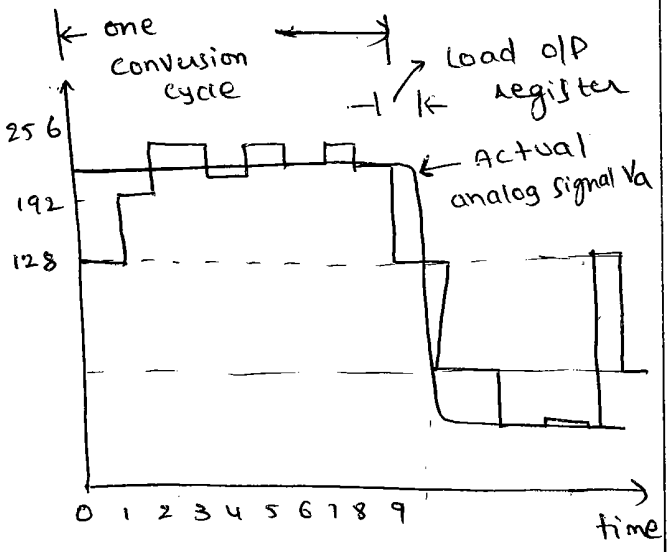


Fig: The D/A output voltage to become successively closer to the actual analog input voltage.

The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

The circuit operates as follows. With the arrival of the start command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now Compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation.

The MSB is left at 1, and the next lower significant bit is made 1 and further tested.

correct digital representation	successive approximation register output V_d at different stages in the Conversion	comparator output
11010100	10000000	1 (Initial o/p)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig (c) : successive approximation conversion sequence for a typical analog input.

However if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.

whenever DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command.

From fig(b) it can be seen that the D/A o/p voltage becomes successively closer to the actual analog i/p voltage. It requires 8 pulses to establish the

accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

Hence for an n-bit DAC, the number of clock pulses required to establish the accurate output is $(2^n + 1)$.

Integrating type ADC's :

1. Dual slope ADC :

Figure below shows the functional diagram of the dual slope or dual ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator.

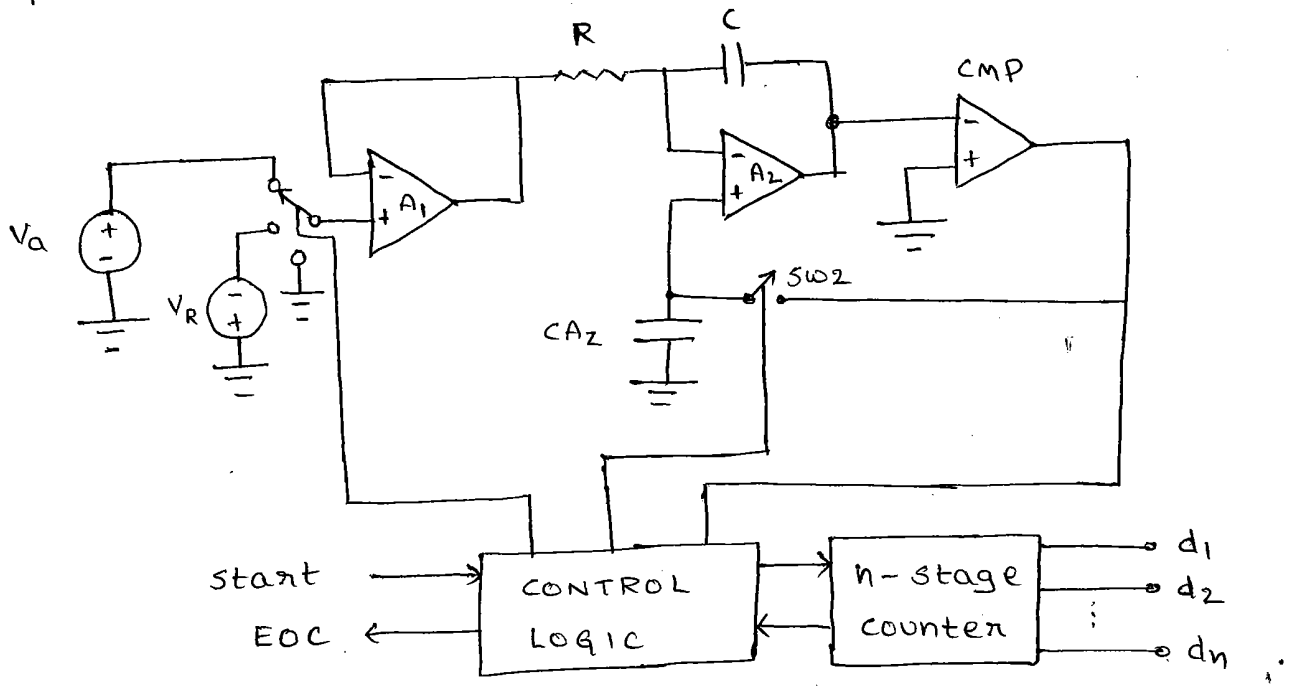
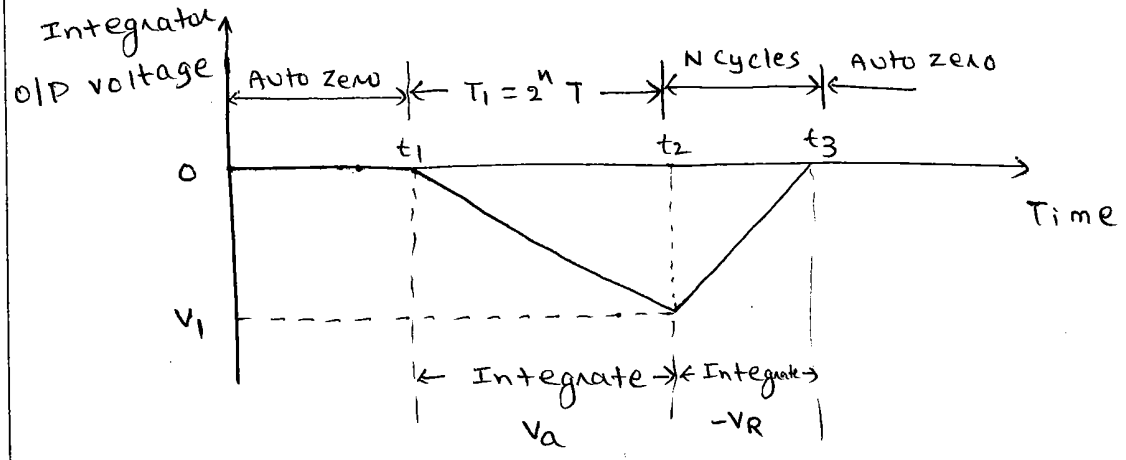


Fig (a) : Functional Diagram of the Dual slope ADC.



Fig(b): Integrated output wave form for the Dual slope ADC.

The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in figure (b). Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.

The circuit operates as follows.

Before the start command arrives, the switch sw1 is connected to ground and sw2 is closed. Any offset voltage present in the A_1, A_2 and comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation

for the input offset voltages of all the three Amplifiers. Later when SW_2 opens C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.

At the arrival of the START command at $t = t_1$, the control logic opens SW2 and connects SW1 to Va and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.

The analog voltage Va is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in fig(b).

The counter resets itself at the end of the interval T_1 and the switch SW1 is connected to the reference voltage $(-V_R)$. The output voltage Vo will now have a positive slope. As long as V_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted.

However, when V_o becomes just zero at time $t = t_3$, the control logic issues and end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3

is proportional to the analog input voltage V_a.

$$T_1 = t_2 - t_1 = 2^n T = \frac{2^n}{\text{clock rate } (f)} \longrightarrow (1)$$

and $$T_2 = t_3 - t_2 = \frac{\text{digital count}(N)}{\text{clock rate}} \longrightarrow (2)$$

For an integrator

$$\Delta V_0 = \left(\frac{-1}{RC}\right) V \Delta t$$

The voltage V_0 will be equal to V_1 at the instant t_2 and can be written as

$$V_1 = \left(\frac{-1}{RC}\right) V_a (t_2 - t_1) \longrightarrow (3)$$

The voltage V_1 is also given by

$$V_1 = \left(\frac{-1}{RC}\right)(-V_R)(t_2 - t_3) \longrightarrow (4)$$

From (3) & (4)

$$V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

From (1) and (2)

$$V_a \frac{2^n}{\text{clock rate}} = V_R \frac{N}{\text{clock rate}}$$

$$\therefore V_a = V_R \left(\frac{N}{2^n}\right)$$

Here since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is indep... of ... and T

Problem: A dual slope ADC uses a 16 bit counter and a 4 MHz clock rate. The maximum input voltage is +10V, the maximum integrator output voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution:

Time period $t_2 - t_1 = \frac{2^n}{\text{clock rate}} = \frac{2^{16}}{4M} = 16.38 \text{ ms}$

For the integrator

$$\Delta V_0 = \left(\frac{-1}{RC}\right) V_a \ (t_2 - t_1)$$

$$\Delta V_0 = V_1 = -8; \quad V_a = 10 \text{ V}$$

$$RC = -\left(\frac{10}{-8 \text{ V}}\right) = 20.47 \text{ ms}$$

$$R = \frac{20.47 \text{ ms}}{0.1 \mu F} = 204.7 \text{ K}\Omega = 205 \text{ K}\Omega$$

Problem: If the analog signal V_a is 4.129 V in the above example, find the equivalent digital number.

Solution: since $V_a = V_R \left(\frac{N}{2^n}\right)$

So the digital count $N = \left(\frac{V_a}{V_R}\right) 2^n$

$$N = 2^{16} \times \frac{10}{8}$$

$N = 33825$, for which the binary equivalent is **1000010000100001**

DAC | ADC Specifications:

Both DAC and ADC are available with wide range of specifications. the various important specifications of converters generally specified by the manufacturers are analysed.

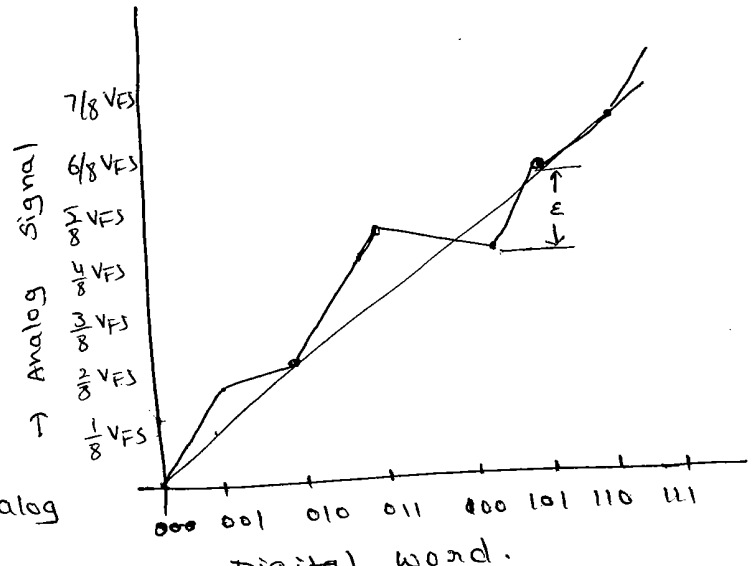
1. **Resolution:** the Resolution of a Converter is the smallest change in voltage which may be produced at the output of the converter. For ex

For example an 8-bit D/A Converter has $2^8 - 1 = 255$ intervals (equal). Hence the smallest change in output voltage is $\frac{1}{255}$ of the full scale output range. In short

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment.}$$

Similarly the resolution of an A/D Converter is defined as the smallest change in analog input for a one bit change at the output.

(2) **Linearity:** The Linearity of an A/D or D/A converter is an important measure of its accuracy. and it tells us how close the Converter output to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the ~~digital~~ analog output and the transfer curve



However in the actual DAC, output voltages do not fall on a straight line because of gain and offset errors - the static performance of a DAC is determined by fitting a straight line through the measured output points. the linearity error measures the deviation of the actual output from the fitted line.

3) Accuracy : Absolute Accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed.

4) Monotonicity :

A monotonic DAC is the one whose analog output increases for an increase in digital input.

Fig shows the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010.

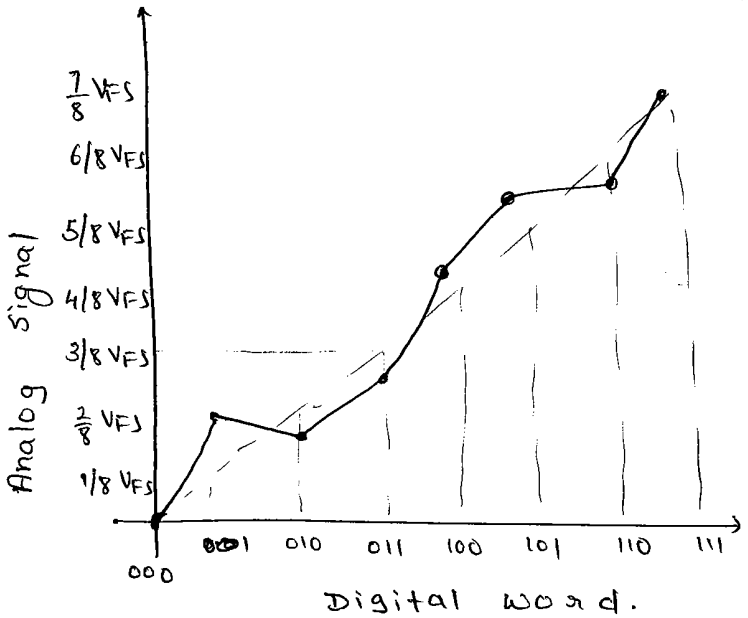


Fig: A Non monotonic 3-bit DAC

A monotonic DAC characteristic is essential in control applications, otherwise oscillations can result.

If a DAC has to be monotonic, the error should be less than $\pm \frac{1}{2}$ LSB at each output level

5) settling time: Settling time represents the time it takes for the output to settle with in a specified band $\pm \frac{1}{2}$ LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitary due to internal parasitic capacitances and inductances.

6) stability: the performance of converter changes with temperature, age and power supply variations. so all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

Problem:

1. How many levels are possible in a two-bit DAC? what is its resolution if the output range is 0 to 3V?

Solution: Levels $= 2^2 = 4$ levels $\left[\because n=2\right)$

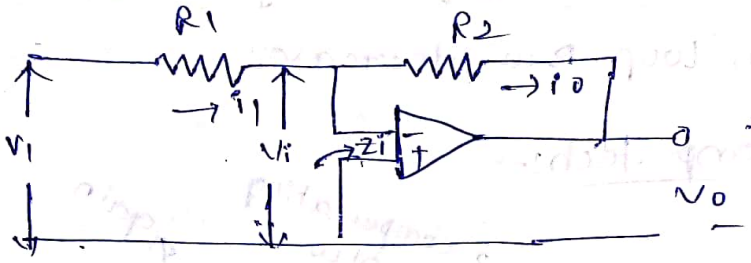
$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{3}{3} = 1\,V$$

Unit-III

Applications of op-amp

inverting diff op-amp:

→ let a voltage v_1 apply to the inverting i/p terminal of op. to a resistor R_1 with the non inverting terminal is



grounded. i.e. -ve F.B. will be provided through resistor R_2. let v_i and v_o denotes the i/p and o/p voltages there will be 180° phase shift b/w v_o and v_i.

→ The overall gain of the amp is given as v_o/v_1 with Z_i is the i/p impedence, due to the virtual ground there is no current flows into the amp. ∴ current through resistor R_1 should be equals to current through resistor R_2 i.e., $i_1 = i_0$.

$$\frac{V_1 - V_i}{R_1} = \frac{V_i - V_o}{R_2}$$

$$\frac{V_1}{R_1} - \frac{V_i}{R_1} = \frac{V_i}{R_2} - \frac{V_o}{R_2}$$

$$\frac{V_o}{R_2} = \frac{V_i}{R_1} + \frac{V_i}{R_2} - \frac{V_1}{R_1} \quad \text{--- (1)}$$

we have the o/p voltage $V_o = -A V_i$

where A is open loop gain sub V_i in the above eq

$$\therefore \frac{V_o}{R_2} = V_i\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_1}{R_1}$$

$$\frac{V_o}{R_2} = -\frac{V_o}{A}\left(\frac{R_1 + R_2}{R_1 R_2}\right) - \frac{V_1}{R_1}$$

$$\frac{V_o}{R_2} + \frac{V_o}{A}\left(\frac{R_1 + R_2}{R_1 R_2}\right) = -\frac{V_1}{R_1}$$

$$V_o\left[\frac{1}{R_2} + \frac{R_1 + R_2}{A R_1 R_2}\right] = -\frac{V_1}{R_1}$$

$$V_o\left[\frac{A R_1 R_2 + R_1 R_2 + R_2^2}{A R_1 R_2^2}\right] = -\frac{V_1}{R_1}$$

$$\frac{V_o}{V_1} = \frac{-A R_1 R_2^2}{R_1[A R_1 R_2 + R_1 R_2 + R_2^2]} \Rightarrow = \frac{-A R_2^2}{R_2[A R_1 + R_1 + R_2]}$$

$$\boxed{\frac{V_o}{V_1} = \frac{-A R_2}{[A R_1 + R_1 + R_2]}} \quad -(2)$$

→ In practice, the typical values of V_o, A, R_1, R_2 the 1st term of eq ② becomes negligibly small as compared to the 2nd term hence it can be ignore.

∴ The closed loop gain $\frac{V_o}{V_1} = -\frac{R_2}{R_1}$

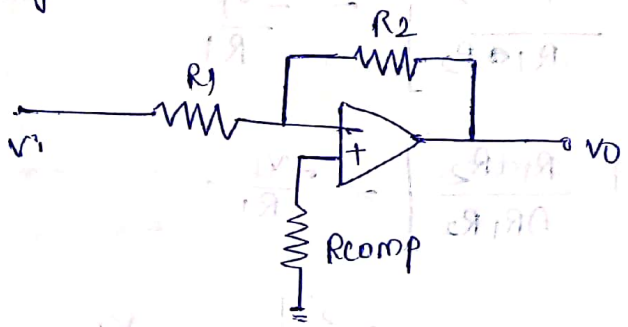
if $R_1 = R_2$ the closed loop gain equal to −1

→ It implies that the o/p has same magnitude as the i/p signal but it is out of phase by 180°.

∴ This op-amp is called "inverter."

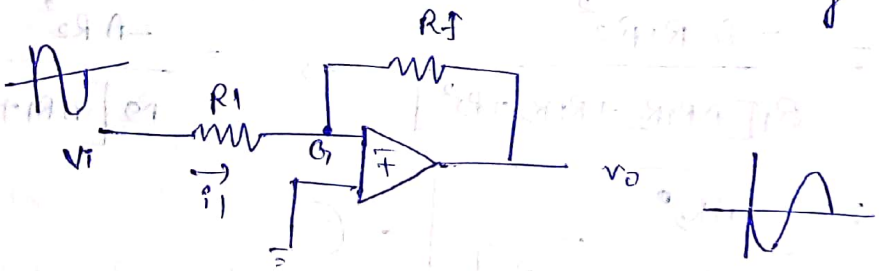
→ If the ratio $R_2/R_1 > 1$ The ckt is termed as "scale changer."

→ In order to provide for o/p bias current compensation it is usually to incorporate resistor $R_{comp} = R_1 \| R_2$ b/w the noninverting i/p terminal and the ground as shown in fig.



op-amp acts as inverting amp:-

→ An inverting amp as shown in fig



→ A weak signal vi is apply is the inverting i/p terminal and vo is the o/p voltage with phase inversion which is it is essential that noninverting terminal is grounded.

→ Due to the virtual ground the current does not enter into the op-amp for all practical applications current through R_1 is equal to the current through Rf resistive Rf.

∴ $I_1 = I_0$.

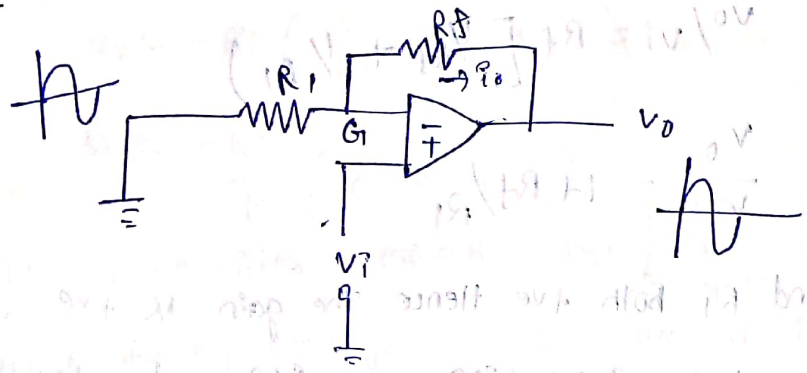
$$\frac{V_i}{R_1} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f}$$

$$\boxed{\frac{V_i}{R_1} = \frac{-V_o}{R_f}} \Rightarrow \boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_1}}$$

Here R_1 and R_f are external resistance for this type of amp the closed loop gain depends only on the F.B resistor R_1 and R_f. By properly choosing R_1 & R_f any desired gain can be obtained.

→ It is seen that there is phase inversion b/w the i/p & o/p voltages. Hence the name is inverting amp.

op-amp acts as noninverting amp:-



→ In this type of op-amp the i/p signal v_i to be applied without phase inversion to the noninverting i/p terminal and inverting i/p terminal grounded through resistor R_1 as shown in fig.

→ R_f is the F.B resistance due to the virtual no current flows into op-amp at G no current towards to the opamp the potential due to G may be assumed to '0'. v_i.

∴ The current through R_1 = current through R_f.

→ R_f is the F.B resistance due to the virtual no current flows into the op-amp at G towards to the op-amp the potential due to G may be assumed to v_i.

the current flows through R_1 = current flows through R_f

$i_1 = i_0$

$$\frac{0 - V_i}{R_1} = \frac{V_1 - V_0}{R_f}$$

$$\frac{-V_i}{R_1} = \frac{V_i - V_0}{R_f}$$

$$\frac{-V_i}{R_1} - \frac{V_i}{R_f} = -\frac{V_0}{R_f}$$

$$V_0/R_f = \text{lcm}\ V_i\left[1/R_f + 1/R_1\right]$$

$$V_0/V_i = R_f\left[1/R_f + 1/R_1\right]$$

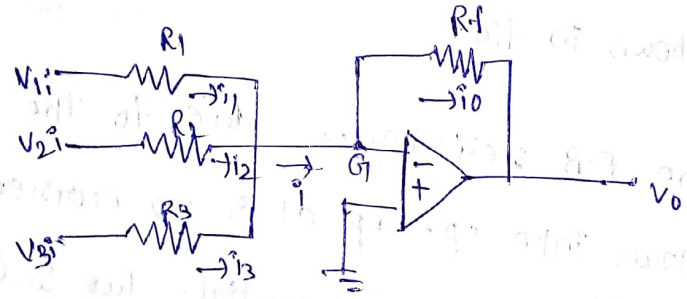
$$\frac{V_0}{V_i} = 1 + R_f/R_1$$

→ Here R_f and R_1 both +ve hence the gain is +ve.

→ There is no phase inversion b/w i/p and o/p voltages

→ The voltage gain always greater than unity.

op-amp acts as a inverting adder (or) summing adder



→ A summing amp the o/p voltage is the sum of all the i/p voltages with the -ve sign it also termed as inverting adder

→ several i/p voltages V_1, V_2, V_3 are apply to the inverting i/p of the op-amp through resistors R_1, R_2 & R_3, as shown in fig.

keeping the non inverting terminal is grounded.

→ If I denotes the i/p current we have $I = I_1 + I_2 + I_3$

Because the virtual ground at G, The current through F.B resistor Rf. should be equals to current through the op-amp.

i.e $I = I_0$.

$$i_1 + i_2 + i_3 = i_0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{0 - V_0}{Rf}$$

$$V_0 = -Rf \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

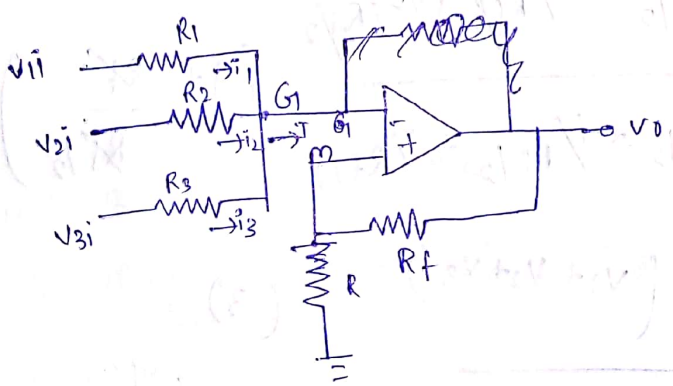
$$V_0 = -\frac{Rf}{R} \left(V_1 + V_2 + V_3 \right)$$

→ If we consider $Rf = R$ then $\boxed{V_0 = -(V_1 + V_2 + V_3)}$

Hence the o/p voltage is the sum of i/p voltages with -ve sign. Hence the name is inverting adder.

Non-inverting summing amplifier:-

⇒ A non inverting amp as shown fig.



→ let the voltage at the inverting i/p terminal will be Vm. because of the virtual ground at the i/p terminals the voltage at G1 also Vm. applying KCL to the node G.

we have $\frac{V_1 - V_m}{R_1} + \frac{V_2 - V_m}{R_2} + \frac{V_3 - V_m}{R_3} = 0$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_m\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]$$

$$V_m = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}$$

→ The op-amp along with the resistors R and Rf. act as non inverting amp.

∴ closed loop gain $V_o/V_m = 1 + \frac{R_f}{R}$.

Substituting for V_m in the above expression we get

$$V_o = V_m\left(1 + \frac{R_f}{R}\right)$$

$$= \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}\left(1 + R_f/R\right)$$

let $R_1 = R_2 = R_3 = R = R_f/2$.

$$\therefore V_o = \frac{V_1/R_f/2 + V_2/R_f/2 + V_3/R_f/2}{1/R_f/2 + 1/R_f/2 + 1/R_f/2}\left(1 + \frac{R_f}{R_f/2}\right)$$

$$= \frac{2/R_f\left(V_1 + V_2 + V_3\right)}{2/R_f(1+1+1)} \quad (3)$$

$$= \frac{V_1 + V_2 + V_3}{3} \quad (3)$$

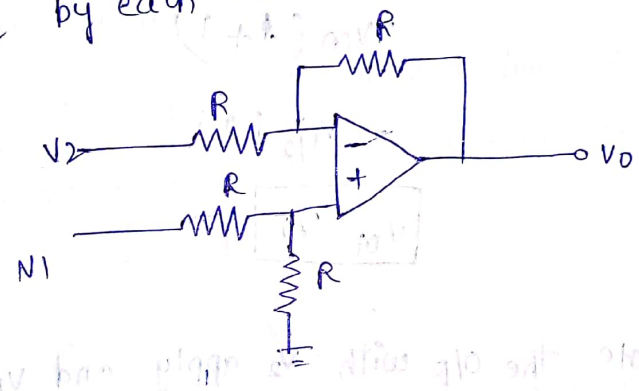
$$\boxed{V_o = V_1 + V_2 + V_3.}$$

→ The o/p is the sum of i/p voltages without change of time Hence the name is non inverting summing amp.

op-amp act as subtractor:-

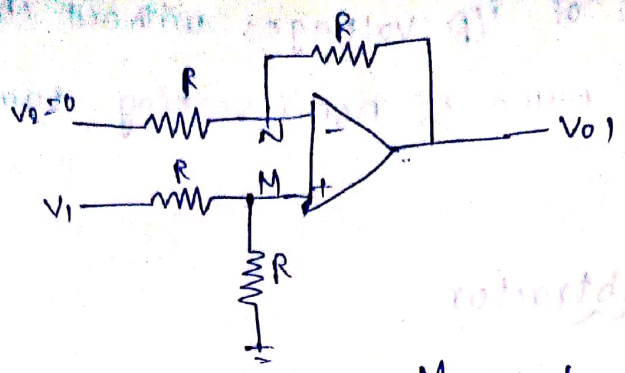
→ The op-amp function has a subtractor giving an o/p voltage with the diff of i/p voltages. The ckt is mainly a basic diff amp in which all resistors are all are equal magnitude is the o/p of the amp can be calculated on the basis of Superposition principle.

principle:- The current through (or) voltage across as element in a linear bilateral nlw equals to the algebric sum of currents (or) voltages produce independently by each source.



→ V_1, V_2 are the i/p voltages at the noninverting and inverting terminals respectively. From the ckt o/p voltage $\boxed{V_o = V_1 - V_2}$.

case i:- let V_{o1} denote the o/p with V_1 apply and V_2 said equal to zero. The ckt modifies as shown.



→ let the potential of node M will be V_m.

$\therefore V_m = V_1 (R/R+R)$

By using potential devided principle

$V_m = V_1/2$

→ The ckt is non inverting amp with an i/p $V_1/2$ at the non inverting terminal and the inverting i/p terminal is grounded through resistor R.

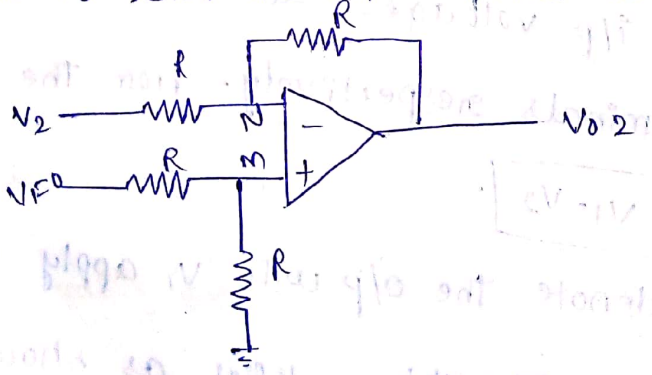
$\therefore$ The o/p voltage $V_{01} = V_m (1 + R/R)$

$= V_m (1+1)$

$= V_1/2 (2)$

$\boxed{V_{01} = V_1}$

Caseii:- let V_{02} denote the o/p with V_2 apply and V_1 is said equal to zero. The ckt modifies as shown in fig.



→ The ckt is basically an inverting amp whose o/p is V_{02}.

$V_{02} = -R_f/R \; V_2 = -R/R \; V_2$

$\boxed{V_{02} = -V_2}$

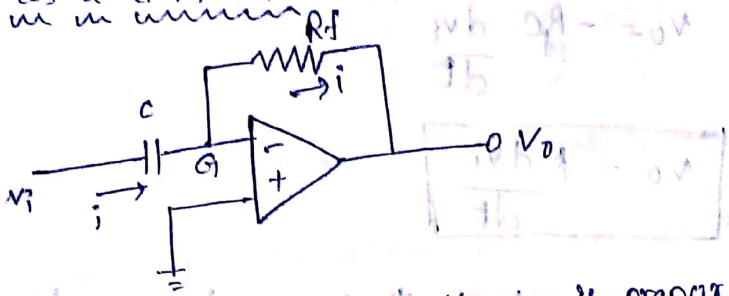
→ when both i/p's V_1 and V_2 are applied we have by the principle of superposition

$$V_0 = V_{01} + V_{02}$$

$$\boxed{V_0 = V_1 - V_2}$$

Hence the op-amp acts as a subtractor.

op amp acts as a differentiator :-



→ In this type of op amp the o/p voltage is proportional to the 1st derivative of the i/p voltage.

→ From the ckt the i/p voltage V_i is apply to the inverting i/p of the op-amp through a capacitor C with noninverting i/p terminal is grounded.

→ let V_0 denotes the o/p voltage. The o/p is connected back through the i/p at G. Through the F.B resistor Rf. The voltage V_i is apply to the capacitor it can charge if Q is the charge on the capacitor.

$\therefore C = Q/V_i$ (i) $V_i = q/C$

→ Differentiating V_i w.r.to time we get $\frac{dv_i}{dt} = \frac{d}{dt}\left(\frac{q}{C}\right)$

$$\boxed{\frac{dv_i}{dt} = \frac{1}{C}\frac{dq}{dt}}$$

→ let i denotes the charging current because of the virtual ground at G. The current passing through F.B resistor should be equal to current passing through capacitor.

$$\therefore i = \frac{dq}{dt} \quad \text{also } i = \frac{-V_0}{R_f}$$

$$\frac{-v_o}{R_f} = \frac{dq}{dt}$$

The value of the $\frac{dq}{dt}$ sub in the above eqn

$$\frac{dv_i}{dt} = 1/c \cdot \frac{-v_o}{R_f}$$

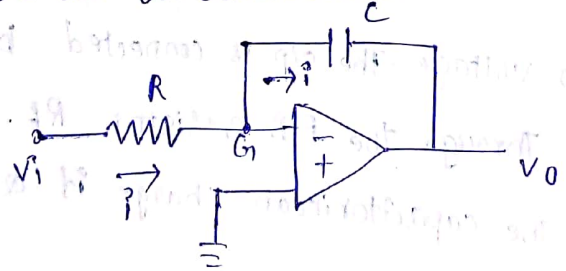
$$v_o = -R_f C \frac{dv_i}{dt}$$

$$\boxed{v_o = K \frac{dv_i}{dt}}$$

→ where K is constant that can be equals to $-R_f C$

∴ The $v_{o/p}$ voltage is praportional to the 1st derivative of the i/p voltage Hence the name is differentiator

op amp can acts as a integrator:-



→ The op-amp may also be used an integrator the op-amp The o/p voltage is praportional to the integral of the i/p voltage.

→ The i/p voltage v_i is apply through a resistor R to the inverting i/p terminal of op-amp. keeping the non inverting i/p terminal is grounded. The o/p is connected back to the i/p through a capacitor C. Because of the virtual ground at G no current flows into the op-amp

→ ∴ The voltage across the capacitor whenever gets charge is equal to $-v_o$. The charge on the capacitor

$q = -CV_o$

at the end of time 't' $-CV_o = \int_0^t i\,dt$

But $i = \frac{V_i}{R}$

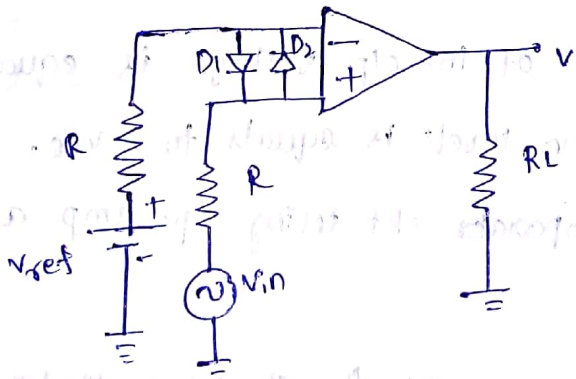
$\therefore -CV_o = \int_0^t \frac{V_i}{R}\,dt$

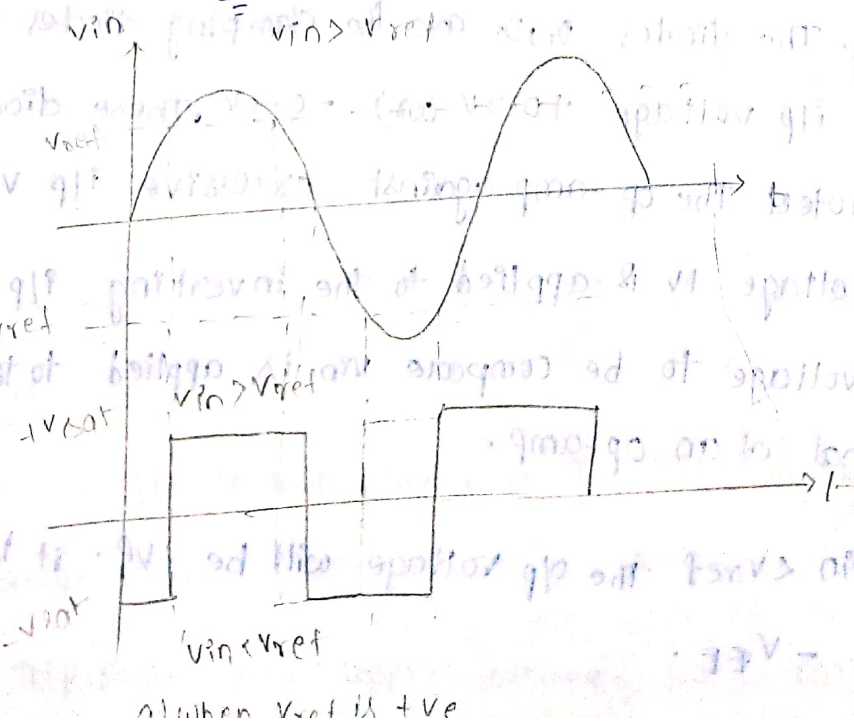
$$V_o = -\frac{1}{RC}\int_0^t V_i\,dt \Rightarrow V_o = K\int_0^t V_i\,dt$$

V_o where R_C is constant

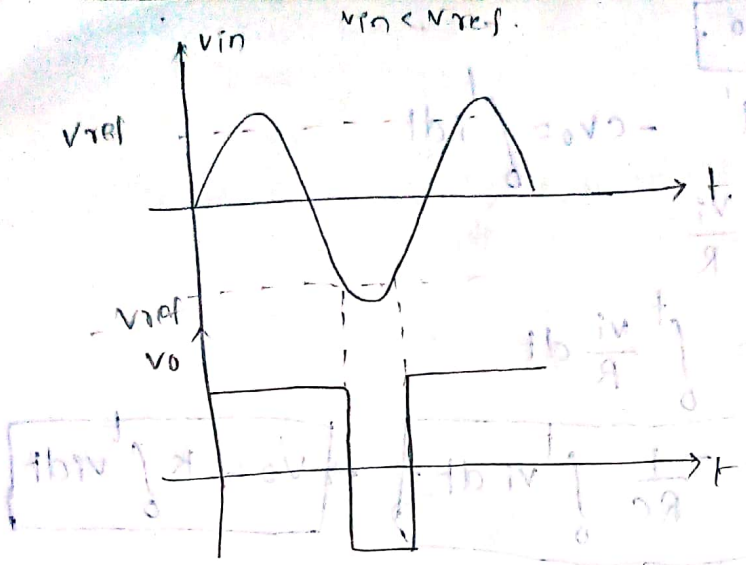
→ From this equ we can seen that the o/p voltage is integral of the i/p voltage Hence the name it's integrator.

op-amp can acts as a comparator:-





when Vref is +ve



b) when Vref is -ve

→ A comparator is a device which compares a signal voltage with a ref voltage. to the inverting i/p terminal this signal ref voltage is applied.

→ The ref volta is to be compared is applied to the other i/p terminal ie non inverting i/p terminal.

→ depending upon the which of the two voltages is grater The o/p is either +ve (or) -ve saturation voltage

→ The +ve saturation level of the o/p voltage is equals to +Vcc. The -ve saturation level is equals to -Vcc.

→ A basic non inverting comparator ckt using op-amp as shown in fig

→ From the fig. The diodes D_1, D_2 are the clamping diodes and they clamp ref i/p voltage +0.7V (or) -0.7V. These diodes are used to protect the op-amp against excessive i/p voltages

→ A ref voltage 1V is applied to the inverting i/p terminal and the voltage to be compare Vin is applied to the noninverting i/p terminal of an op-amp.

→ ∴ Vin < Vref the o/p voltage will be -ve. It is approximately equals to $-V_{EE}$.

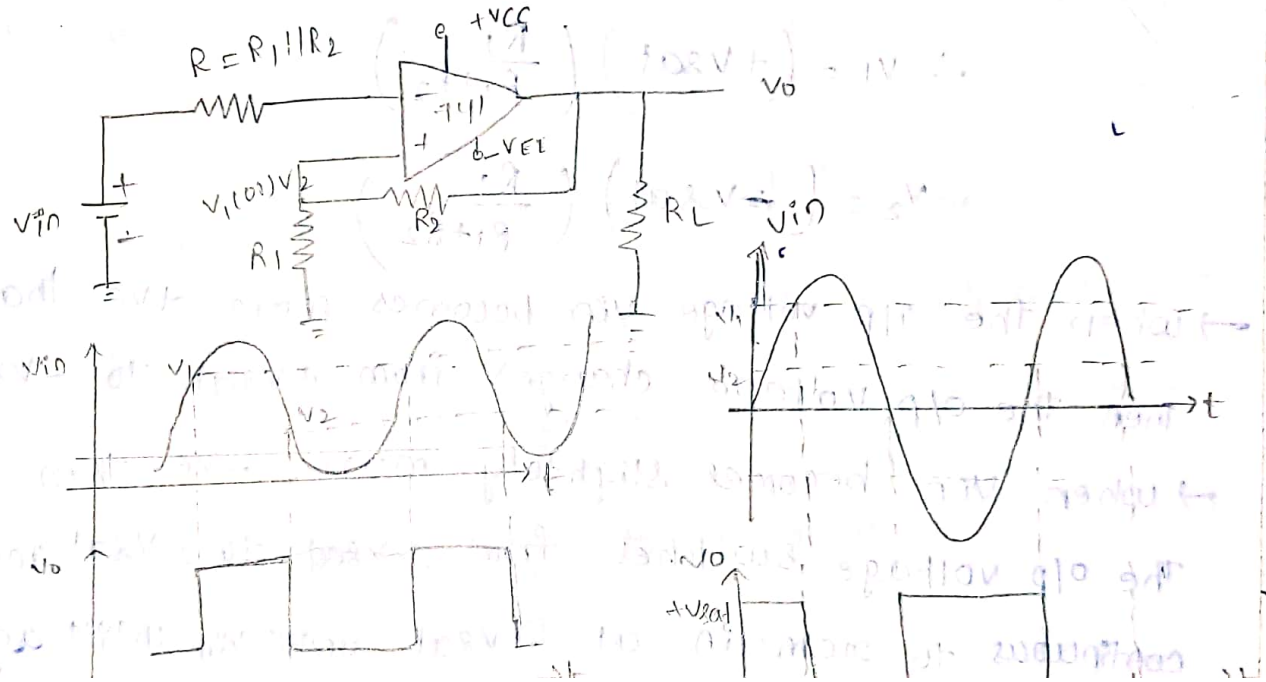
→ If $V_{in} > V_{ref}$ the o/p voltage would be +ve it being approximately equals to +Vcc.

→ When even V_{in} becomes equals to V_{ref}. The o/p voltage V_o changes instantaneously from one saturation level to another level. i.e from +Vcc to $-V_{EE}$ or from $-V_{EE}$ to +Vcc

→ The i/p & o/p waveforms are shown in fig.

→ The comparator sometimes called as voltage level detector."

Schmitt trigger using op-amp :-



(or) lower trip point (or) lower threshold point.

→ The state of the o/p changes in this process the o/p voltage takes the shape of square wave This is graphically shown above.

→ let V_1 = UTP , V_2 = LTP

→ whenever the i/p is sine wave the device would be termed sine wave to square wave converter.

→ An op-amp provides with +ve feed back we can function as schmitt trigger The ckt is shown above.

→ when $V_o = +V_{sat}$ the voltage across R_1 is V_1. when $V_o = -V_{sat}$ the voltage across R_2 is V_2

$$\therefore V_1 = (+V_{sat})\left(\frac{R_1}{R_1+R_2}\right)$$

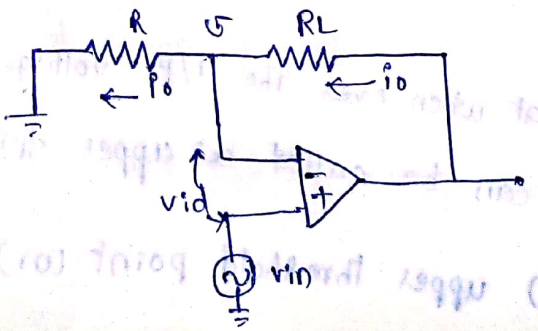
$$V_2 = (+V_{sat})\left(\frac{R_1}{R_1+R_2}\right)$$

→ when the i/p voltage V_{in} becomes more +ve than V_1. Then the o/p voltage changes from $+V_{sat}$ to $-V_{sat}$.

→ when V_{in} becomes slightely more -ve than V_2. The o/p voltage switches from $-V_{sat}$ to $+V_{sat}$ and it continuous to remain at $+V_{sat}$ untill V_{in} untill again reaches the value V_1

→ The i/p and o/p w/fs are shown in the fig.

Op-amp acts as a voltage to current converter:-



→ The op-amp can be used with an advantage of voltage to current converter. In this type of ckt an i/p voltage gets converted into an o/p current The ckt as shown in fig.

→ From the ckt 'vid' is the differential i/p voltage and I_o is the o/p current and R_L is the load resistance.

→ The i/p voltage vin is apply to the noninverting i/p terminal of an op-amp. Because of virtual ground as a i/p terminals practically no current flows into the op-amp. and we have the current through R equal to F.B. element. voltage

→ ∴ F.B element voltage $V_f = i_o \cdot R$.

By applying KVL at node G $V_{in} = V_f$.

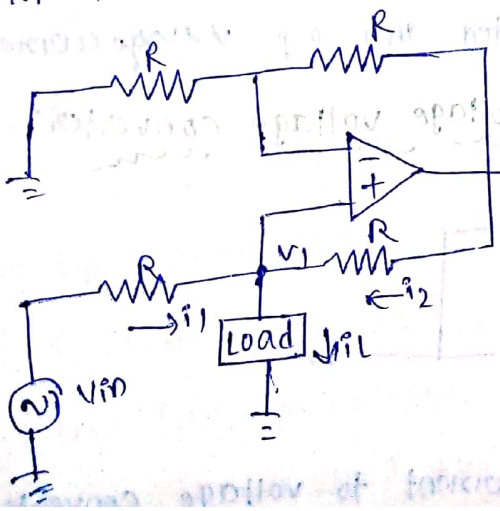
$\therefore V_{in} = i_o R$.

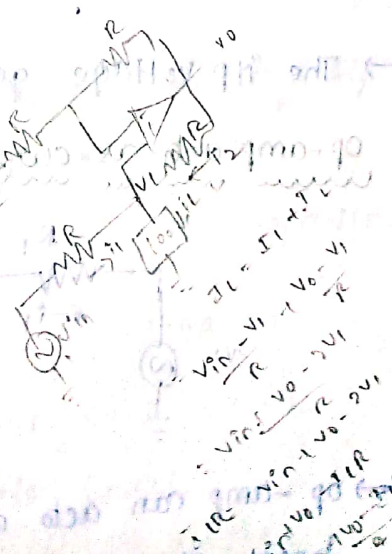
$\therefore i_o = V_{in}/R$ Here R is a fixed value. Hence

The i/p voltage vin gets converted into an o/p current I_o.

∴ The op-amp ckt is called voltage to current converter.

→ The another method of voltage to current is shown in fig This ckt load is grounded.





→ let V_1 denotes the voltage of the non inverting terminal and I_L is the load current.

→ By applying KCL we have $I_L = I_1 + I_2$,

$$= \frac{V_{in} - V_1}{R} + \frac{V_0 - V_1}{R}$$

$$i_L = \frac{V_{in} + V_0 - 2V_1}{R}$$

$$V_{in} + V_0 - 2V_1 = i_L R \Rightarrow V_{in} + V_0 - i_L R = 2V_1$$

$$\boxed{V_1 = \frac{V_{in} + V_0 - i_L R}{2}}$$

→ W.K.T. The closed loop gain of the non inverting op-amp is given as $(1 + R_f/R_1)$.

→ Here all resistors are of equal value.

$$\therefore (1 + R/R) = 2$$

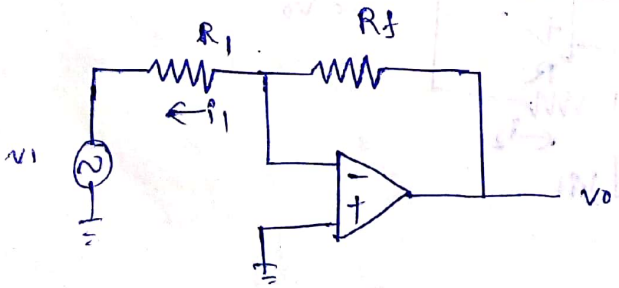
→ ∴ o/p voltage $V_0 = 2V_1$

$$V_0 = 2\left(\frac{V_{in} + V_0 - i_L R}{2}\right)$$

$$\boxed{V_0 = V_{in} + V_0 - i_L R}$$

→ sub/value $V_{in} = i_L R \Rightarrow \boxed{i_L = \frac{V_{in}}{R}}$

→ The i/p voltage gets converted into o/p voltage current, op-amp acts as current to voltage voltage converter:-



→ op-amp can acts as current to voltage converter. The basic ckt is the same for an op amp can acts as a inverting

amp.

→ From this ckt the overall gain of the op-amp is given as

$$\frac{V_0}{V_1} = -R_f/R_1$$

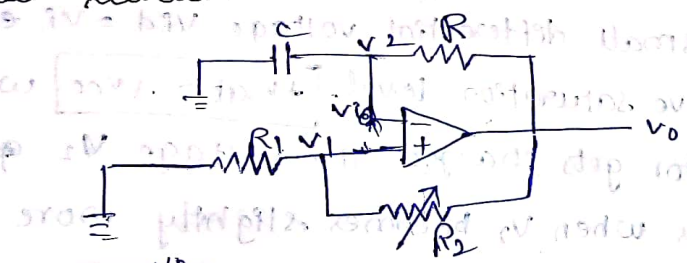
$$V_0 = -\left(V_1/R_1\right) R_f$$

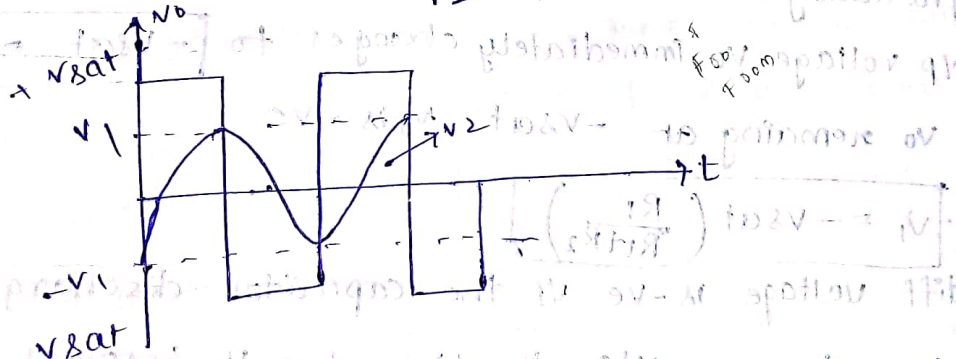
$$\boxed{V_0 = -i_1 \cdot R_f}$$

Here $i_1 = \frac{V_1}{R_1}$

→ Hence the i/p current is converted into an o/p voltage.

Square wave Generator:-





→ The op-amp can function as square wave generator as shown in the figure.

→ From the fig it is seen that the voltage at the noninverting i/p terminal is V_1. The voltage across R_1, the voltage at the inverting i/p terminal is V_2. at the voltage across the capacitor

→ In practice $+V_{sat} = +V_{CC}$ and $-V_{sat} = -V_{EE}$ depending on wheather the diff i/p voltage V_{id} is +ve cor) -ve the op voltage V_0 is -ve cor) +ve, saturation level

let it be assumed that the capacitor is
when the DC supply voltages +Vcc and -VEE are applied
∴ voltage across capacitor is $v_2 = 0$.

~~Square wave generator~~:-

but v_1 is not equal to zero but it has finite value because of offset voltage The actual value of v_1 depends not only on the o/p offset voltage but also the resistors R_1 and R_2 let it be assumed that v_1 is +ve : we have diff voltage

$$v_{id} = v_1 - 0 = v_1$$

→ even though the small differential voltage $v_{id} = v_i$ can drive the op-amp into +ve saturation level. $+V_{sat} = +V_{cc}$ with this voltage the capacitor gets charged The voltage v_2 ~~gradually~~ gradually rises when v_2 becomes slightly more +ve than v_1 The o/p voltage v_o immediately changes to $-V_{sat} = -V_{EE}$

→ with v_o remaing at $-V_{sat}$ v_1 is -ve

$$\therefore v_1 = -V_{sat}\left(\frac{R_1}{R_1+R_2}\right)$$

→ The diff voltage is -ve ~~v~~ the capacitor discharges again charges in the opposite direction when v_2 becomes slightly more -ve than $-v_1$ then op-amp o/p switches to $+V_{sat}$ again

→ This we complete one cycle of the o/p wave

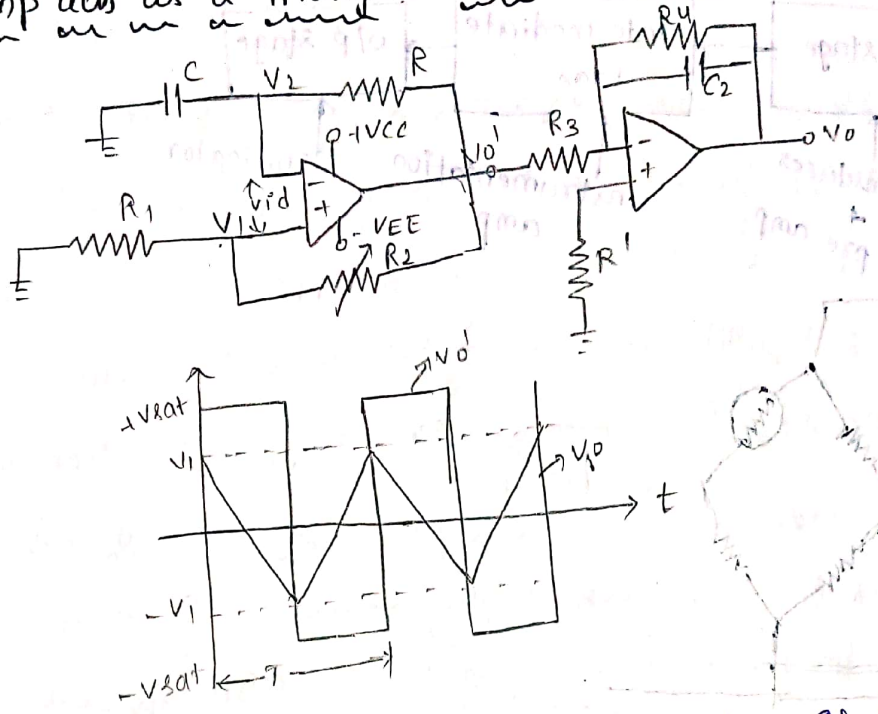
we have $$v_1 = +V_{sat}\left(\frac{R_1}{R_1+R_2}\right)$$

→ ∴ The o/p w/f of v_o to be a square wave . The op-amp can function as a square wave generator which is also referred as astable multivibrator (or) free running oscillato

→ The time period of astable multivibrator is

$$T = 2RC \log_e\left(\frac{2R_1 + R_2}{R_2}\right)$$

Op-amp acts as a triangular wave Generator:-



→ The basic ckt of triangular wave generator as shown in fig. in a it is a series combination of square wave generator ckt and integrator generator ckt.

→ The o/p of the integrator ckt.

$$V_o = \frac{-1}{R_3 C_2} \int v_o' dt$$

i-e, o/p voltage v_o is praportional to time integral of v_o'.

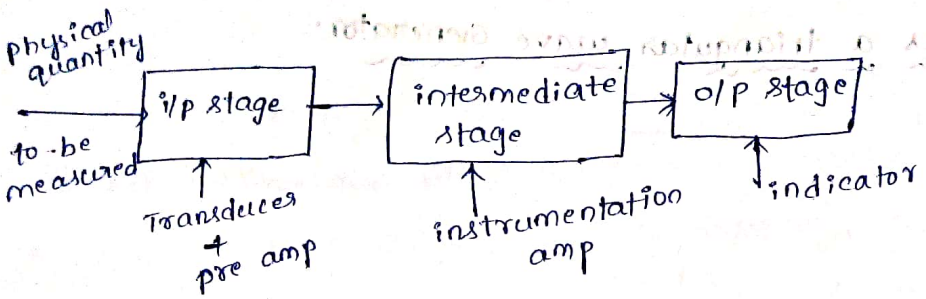
→ The i/p is square wave and o/p wave is triangular.

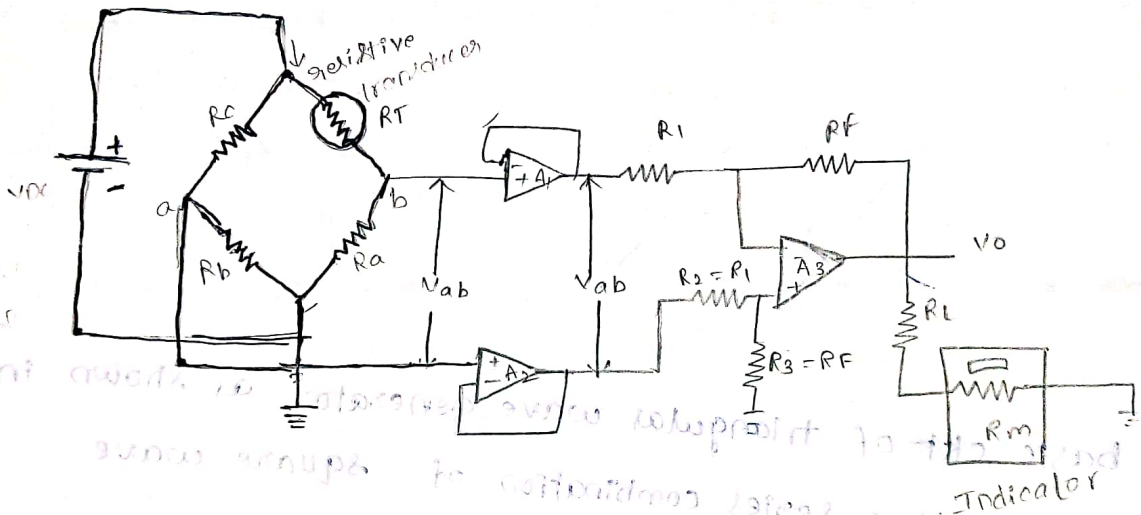
→ In order to get the o/p voltage wave is triangular one general rule will be satisfied is 5 times $R_3 C_2 > T/2$.

where T is timeperiod of i/p square wave and also it is neccessary to shunt the capacitor C_2 by a resistor $R_f = 10R_3$.

→ In order to obtain stable triangular wave

Instrumentation amplifier using op-amp:-





→ The instrumentation amp mainly used in industrial applications The amp is usually prevent by the o/p of a transducer a transducer converts one form of energy into another form of energy for example physical energy into electrical energy

→ The In industrial applications it is necessary to measure the physical quantities like temperature pressure humidity in such condition an instrumentation amp place a major role

→ The block diagram representation of Rumi instrumentation system as shown in fig.

→ The instrumentation amp forms an the intermediate stage of the stage system the main function is amplify the weak o/p signal of the i/p stage. So that the strength

signal can operate an indicator, the indicator is suitably calibrated. It can measure directly the physical quantity.

→ An instrumentation amp which uses a transducer bridge is shown in figure.

→ From the Fig A_1, A_2, A_3 are the op-amps. R_a, R_b, R_c, R_T are the ratio resistive arms. where R_f is the Feed back resistance the transducer used is a resistive transducer of a resistor R_T and it forms one of the ratio arms of the wheatstone bridge.

→ It can be energised by a suitable source in practice the bridge is balanced under desired set conditions said by the designer depending on practical requirement

→ At balancing condition $V_a = V_b$.

$$\frac{R_c}{R_b} = \frac{R_T}{R_a}$$

→ when the physical quantity to be measured the changes The resistance of the transducer changes as a result The bridge becomes unbalanced. let ΔR represents the change in resistance of the transducer.

∴ The new value of resistance equals to $R_T + \Delta R$.

→ let V_{ab} represents voltage across the terminals of the bridge we have $V_{ab} = V_a - V_b$.

But $V_a = V_{dc}\left(\frac{R_a}{R_a + R_T + \Delta R}\right)$

$V_b = V_{dc}\left(\frac{R_b}{R_b + R_c}\right)$

$$V_{ab} = V_{dc}\left(\frac{R_a}{R_a + R_T + \Delta R}\right) - V_{dc}\left(\frac{R_b}{R_b + R_c}\right)$$

$= V_{dc}$

let $R_a = R_b = R_c = R_T = R$

$$V_{ab} = V_{dc}\left(\frac{R}{R+R+\Delta R}\right) - V_{dc}\left(\frac{R}{R+R}\right)$$

$$= V_{dc}\left(\frac{R}{2R+\Delta R}\right) - V_{dc}\left(\frac{R}{2R}\right)$$

$$= V_{dc}\left[\frac{R}{2R+\Delta R} - \frac{R}{2R}\right]$$

$$= V_{dc}\left[\frac{R}{2R+\Delta R} - \frac{1}{2}\right]$$

$$= V_{dc}\left[\frac{2R - (2R+\Delta R)}{2(2R+\Delta R)}\right] = V_{dc}\left[\frac{-\Delta R}{2(2R+\Delta R)}\right]$$

$$\boxed{V_{ab} = V_{dc}\frac{-\Delta R}{2(2R+\Delta R)}}$$

→ This voltage V_{ab} is applied to the instrumentation amp is the combination of 3 operational amp's.

→ where A_1 & A_2 are the voltage followers. Their main function is to eliminate the loading effect the bridge ntw. But we have the gain of the amp A_3 is $\frac{-R_f}{R_1}$.

∴ The V_o o/p voltage $\boxed{V_o = V_{ab}\frac{-R_f}{R_1}}$

sub V_{ab}

$$V_o = V_{dc}\frac{-\Delta R}{2(2R+\Delta R)} - \frac{R_f}{R_1}$$

But ingeneral ΔR is quite small

$\therefore 2R + \Delta R \simeq 2R$

$$V_o = V_{dc} \frac{\Delta R}{2(2R)} \frac{R_f}{R_1}$$

$$\boxed{V_o = V_{dc} \frac{\Delta R}{4R} \frac{R_f}{R_1}}$$

→ In this expression the DC source V_{dc}, R_1, R and R_f having fixed magnitude.

$\therefore$ o/p voltage $\boxed{V_o \propto \Delta R}$

→ The o/p voltage is directly praportional the change in resistance of the transducer and this change in resistance is a measure of the physical quantity involve

→ The o/p voltage V_o can operate an indicating meter which can be calibrated directly interms of the physical quantity being measure.

Ac amplifier:-

→ The applications discussed so far are dealing with both Ac & Dc signals. now we can interact with only Ac signals the Ac amplifiers is used when it is required to get the Ac frequency of an op-amp.

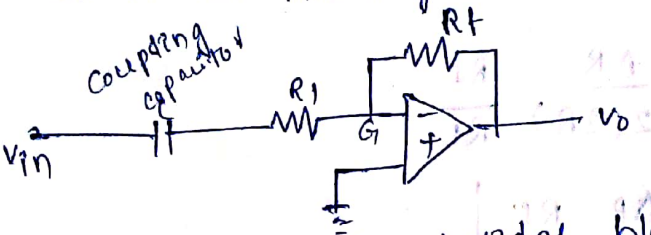
→ It is neccessary to eliminate the Dc components this can be achieve by using an Ac amp with a coupling capacitor.

→ Ac amplifiers are two types

1. Inverting Ac amp
2. Non inverting Ac amplifier

Inverting Ac amplifier:-

→ The ckt of the inverting Ac amp is shown in fig.



→ The coupling capacitor besides blocking the DC component of the i/p and also sets the lower 3dB frequency of the amp with the help of resistor R_1.

→ consider the virtual ground at G. The o/p voltage V_o is given by $\boxed{V_o = -\frac{1}{R_f}}$

$$V_o = -\frac{V_{in}}{R_1 + 1/sC}$$

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1 + 1/sC} \Rightarrow \frac{-R_f sC}{R_1 sC + 1}$$

$$= \frac{-R_f s}{C\left(R_1 s + \frac{1}{C}\right)}$$

$$\frac{V_o}{V_{in}} = \frac{-R_f s}{R_1\left[s + 1/R_1 C\right]}$$

From this eqn the lower cutoff frequency f_L is given by

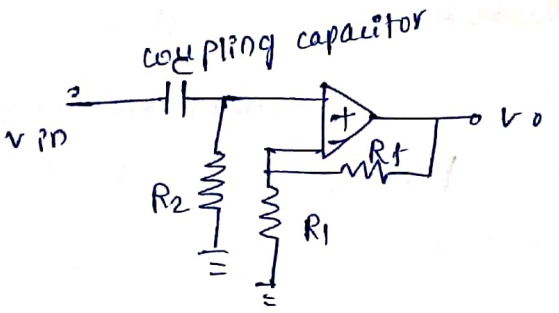
$$f_L = \frac{1}{2\pi R_1 C}$$

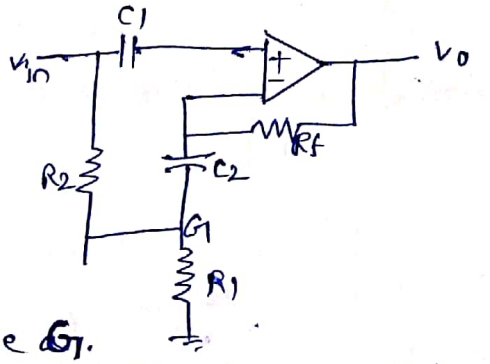
→ The capacitor behaves as a ckt asually in the mid band range of frequencies.

∴ The gain becomes $-R_f/R_1$

Noninverting Ac amp:-

→ The ckt of noninverting Ac amp is shown in fig





→ If R_2 is not connected to node G. but connect to the ground then it will be provide a Dc component to the ground because of this the overall i/p impedence of the amp reduces.

→ This prblm is rectified by connecting the capacitor C_1 as shown in fig. The capacitor C_1 this act as short ckt to ac signals.

→ The Resistance R_2 carries no current when node G and noninverting terminal R_f same potential this can improves the i/p impedence of the ckt.

log amplifier:-

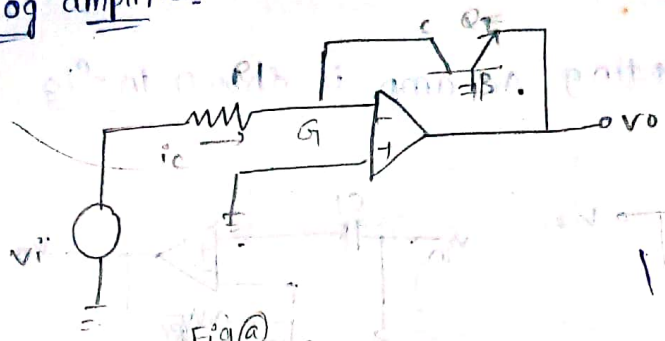


Fig @

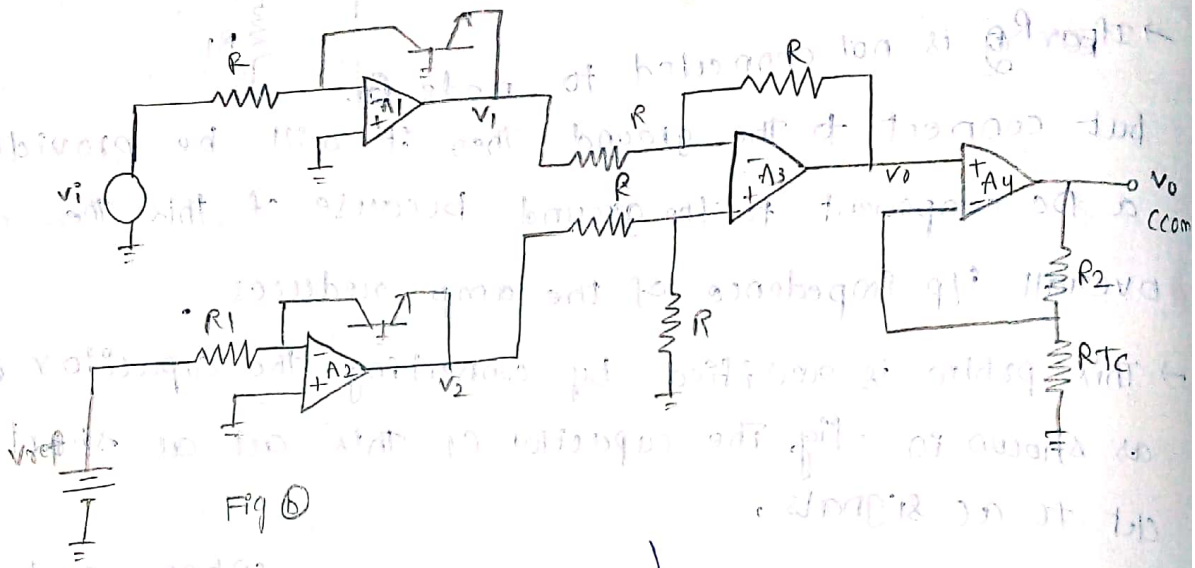


Fig (b)

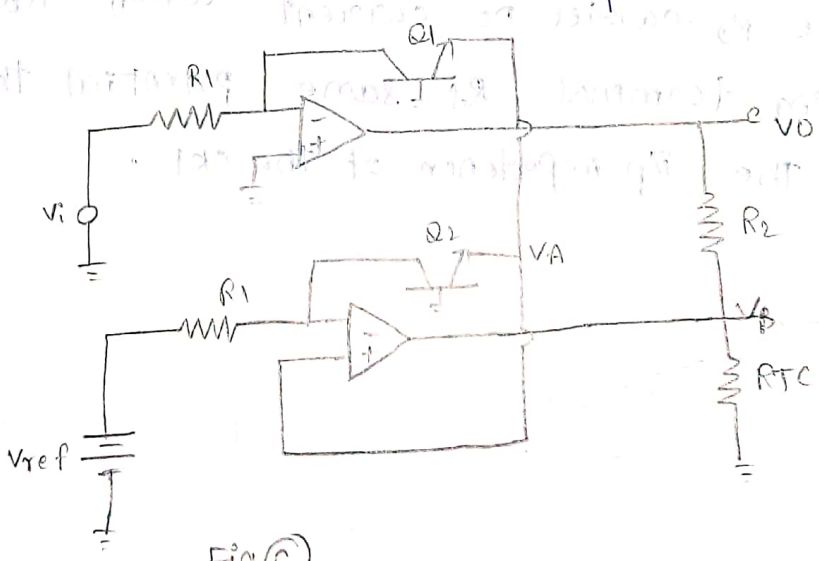


Fig (c)

→ log amp and @ antilog amp are used in many application in practice The o/p voltage of log amp is proportional to the logarithmic of the i/p voltage. The diode current eqn forms the basic principle of operation of a log amp

→ The diode current eqn may be expressed

$$I_D = I_S [e^{qv/KT} - 1]$$

where I_D = current through the diode

I_S is reverse saturation current

Q is charge on electron i.e, 1.6×10^{-19} coloumbs

V_{BE} the voltage applied across the diode

k is boltzman constant i.e, 1.38×10^{-23} Joules/kelvin

T is obsolute temperature

→ consider the basic log amp. ckt as shown in fig@

→ The ckt uses a grounded base transistor Q in the F.B path the collector terminal is connected to the inverting i/p of the op-amp. since the non inverting i/p terminal is grounded because of the virtual ground at 'G' The potential at collector terminal becomes '0'.

→ since both base and collector terminals are grounded

∴ The transistor can be visualise as a diode

∴ The diode current eqn is applicable.

→ ∴ From the ckt

$$I_E = I_S \left(e^{qV_E/KT} - 1\right)$$

But $I_E = I_C$ when base is grounded

$$I_C = I_S \left(e^{qV_E/KT} - 1\right)$$

$$I_C/I_S = e^{qV_E/KT} - 1$$

$$\frac{I_C}{I_S} + 1 = e^{qV_E/KT}$$

→ Since $I_C > I_S$

$$\frac{I_C}{I_S} = e^{qV_E/KT}$$

$$\frac{qV_E}{KT} = \log_e\left(\frac{I_C}{I_S}\right)$$

$$V_E = \frac{KT}{q} \log_e\left(\frac{I_C}{I_S}\right)$$

→ From the ckt diagram we have $I_C = \frac{V_i}{R_1}$ sub the value of I_C in the above expression

$$V_E = \frac{KT}{q} \log_e \left(\frac{V_i}{R_1 I_S}\right)$$

→ From the ckt the o/p voltage $V_o = -V_E$

Let $R_1 I_S = V_{ref}$

$$\boxed{V_o = \frac{-KT}{q} \log_e \left(\frac{V_i}{V_{ref}}\right)}$$

→ In the above expression for V_o the value of k, T and q are fix and also V_{ref} can be kept constant.

$$\boxed{\therefore V_o \propto \log(V_i)}$$

→ From this expression the o/p voltage is praportional to logarithum of the i/p voltage. for this reason this ckt is called "log amp".

→ This expression may also be written as

$$V_o = \frac{-KT}{0.4343q} \log_{10}\left(\frac{V_i}{V_{ref}}\right)$$

→ In order to the above relationship holds good it is essential that V_{ref} is constant we have $V_{ref} = R_1 I_S$.

→ hence the reverse satusation current I_S should remain constant but I_S is found to vary from transistor to another transistor also I_S is temperature dependent Thus it may not be possible in practice it can be obt a stable ref voltage.

→ In order to obey this difficulty the ckt is modi to the modified ckt are shown in fig(b) and (c)

→ from the fig(b) the ckt uses four op-amps. The P/p signal V_i is applied to the op-amp A1 and the ref voltage. V_{ref} is applied to the op-amp A_2 both op-amps A1 and A_2 are integrated in a close ckt on the same silicon va. wafer. So that the reverse saturation current match at all temperatures.

→ $\therefore I_{S1} = I_{S2} = I_S$,

→ For op amp A1, The o/p voltage $V_1 = \frac{-KT}{q} \log\left(\frac{V_i}{R_1 I_S}\right)$

$$V_2 = -\frac{KT}{q} \log\left(\frac{V_{ref}}{R_1 I_S}\right)$$

→ These 2 o/p forms i/ps to op-amp A3 to the o/p V_o is diff of the i/p's.

$$V_o = V_2 - V_1$$

$$= -\frac{KT}{q} \log\left(\frac{V_{ref}}{R_1 I_S}\right) + \frac{KT}{q} \log\left(\frac{V_i}{R_1 I_S}\right)$$

$$= \frac{KT}{q} \log\left(\frac{V_i}{V_{ref}}\right)$$

→ Since V_{ref} is not dependent and temperature and it is fixed value in magnitude from the above expression.

→ The o/p voltage V_o is still dependent on 'T'.

∴ This dependent of V_o is applied to the non inverting terminal of A_4 which provides a non inverting gain of $\left(1 + \frac{R_2}{R_{TC}}\right)$

where R_{TC} = a temperature sensitive resistance with +ve coefficient it is also called 'sensistor'.

→ ∴ The o/p of op-amp A4 = $v_{o(comp)} = \left(1+\frac{R_2}{RTC}\right)\frac{KT}{q}\log\left(\frac{V_i}{V_{ref}}\right)$

→ From this expression RTC helps to maintain the slope of the eqn of $v_{o(comp)}$ constant at all temperatures.

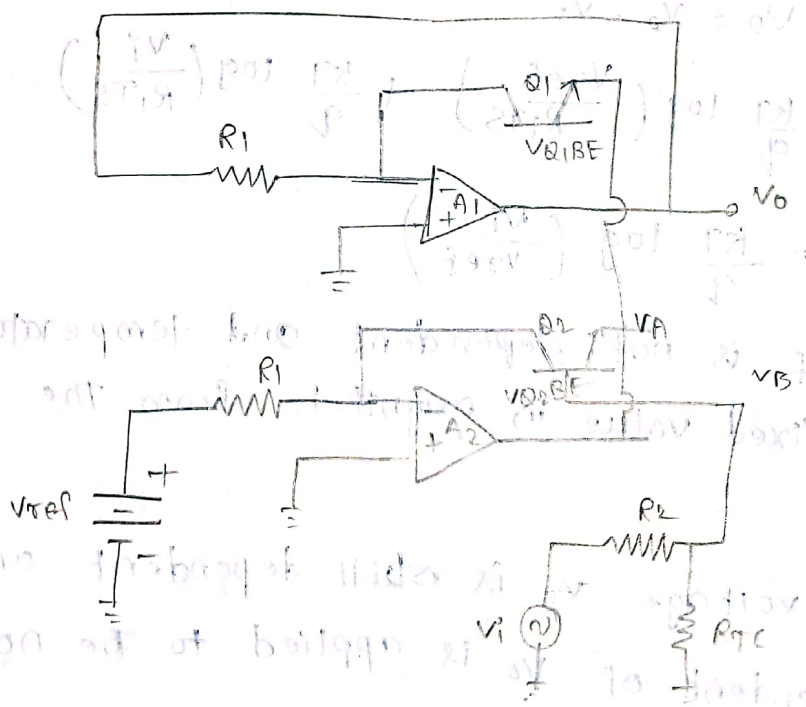
→ ∴ V_o compensation $\propto \log(V_i)$

→ Another modified ckt which uses only two op-amps as shown in fig c.

→ from this modified ckt the o/p voltage is given by the same expression but there is a phase inversion.

→ $v_{o(comp)} = -\left(1+\frac{R_2}{RTC}\right)\frac{KT}{q}\log\left(\frac{V_i}{V_{ref}}\right)\left(1+\frac{R_2}{RTC}\right)$

Antilog amp:-



→ The i/p voltage v_i is applied to the base of the transistor Q_2 via the potential devider arrangement of R_2, RTC. The o/p voltage V_o of the antilog amp is fed back to the inverting i/p terminal of op-amp A1 we have $V_{Q1BE} = \frac{KT}{q}\log_e\left(\frac{V_o}{R_1 I_S}\right)$

$\left(1+\frac{R_2}{R_{TC}}\right)$ $V_{Q_2BE} = \frac{KT}{q}\log_e\left(\frac{V_{ref}}{R_1 I_S}\right)$

also $V_i = -V_{Q_1BE}$ since the base of the transistor Q_1 is grounded.

$$\therefore V_i = -\frac{KT}{q}\log_e\left(\frac{V_0}{R_1 I_S}\right)$$

→ The potential at $V_B = V_i\left(\frac{R_{TC}}{R_2+R_{TC}}\right)$.

By using potential divider rule. But V_B is the voltage at the base of the transistor Q_2.

∴ The emitter voltage of the transistor Q_2 is equal to

$$V_A = V_B - V_{Q_2BE}.$$

$$-\frac{KT}{q}\log\left(\frac{V_0}{R_1 I_S}\right) = V_i\left(\frac{R_{TC}}{R_2+R_{TC}}\right) - \frac{KT}{q}\log_e\left(\frac{V_{ref}}{R_1 I_S}\right)$$

$$V_i\frac{R_{TC}}{R_2+R_{TC}} = -\frac{KT}{q}\log\left(\frac{V_0}{R_1 I_S}\right) + \frac{KT}{q}\log_e\left(\frac{V_{ref}}{R_1 I_S}\right)$$

$$V_i\frac{R_{TC}}{R_2+R_{TC}} = -\frac{KT}{q}\left[\log_e\left(\frac{V_0}{R_1 I_S}\right) - \log_e\left(\frac{V_{ref}}{R_1 I_S}\right)\right]$$

$$-\frac{KT}{q}\log_e\left(\frac{V_0}{V_{ref}}\right) = V_i\frac{R_{TC}}{R_2+R_{TC}}.$$

$$\log_e\left(\frac{V_0}{V_{ref}}\right) = -\frac{q}{KT}V_i\left(\frac{R_{TC}}{R_2+R_{TC}}\right)$$

0.4343 is multiplied on both sides of the expression

$$0.4343\log_e\left(\frac{V_0}{V_{ref}}\right) = -0.4343\frac{q}{KT}V_i\frac{R_{TC}}{R_2+R_{TC}}.$$

where $0.4343\log_e\left(\frac{V_0}{V_{ref}}\right) = \log_{10}\left(\frac{V_0}{V_{ref}}\right)$

~~$0.4343\log_e\left(\frac{V_0}{V_{ref}}\right)$~~ =

$$\log_{10}\left(\frac{V_o}{V_{ref}}\right) = -kV_i$$

$\left[\log_e x = \frac{\log_{10} x}{\log_{10} e}\right]$

where $k = 0.4343 \frac{q}{kT}$ $\frac{RTC}{R_2 + RTC}$

$\log_e x = \frac{\log_{10} x}{0.4343}$

$0.4343 \log_e x = \log_{10} x$

$$\frac{V_o}{V_{ref}} = 10^{-kV_i}$$

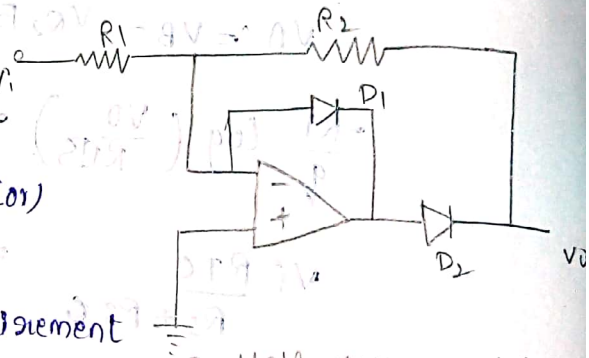
$$V_o = V_{ref}\, 10^{-kV_i}$$

→ Since Vref is of constant magnitude from this relationship it is concluded that an increase of i/p voltage by 1 volt as a result decrease of 10v in the o/p voltage. Then the ckt can function as antilog amp.

Precision Rectifiers :-

→ precision rectifiers are required if the voltages less than threshold voltage for example few millivolts (or) micro volts.

→ An op amp ideally fulfills the requirement



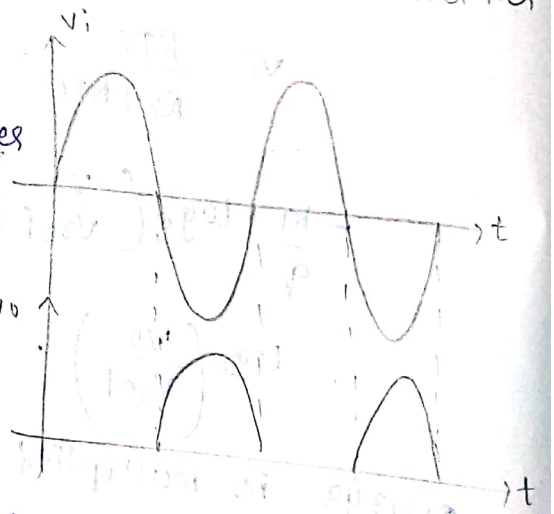
a. Half wave rectifier

precision halfwave rectifier :-

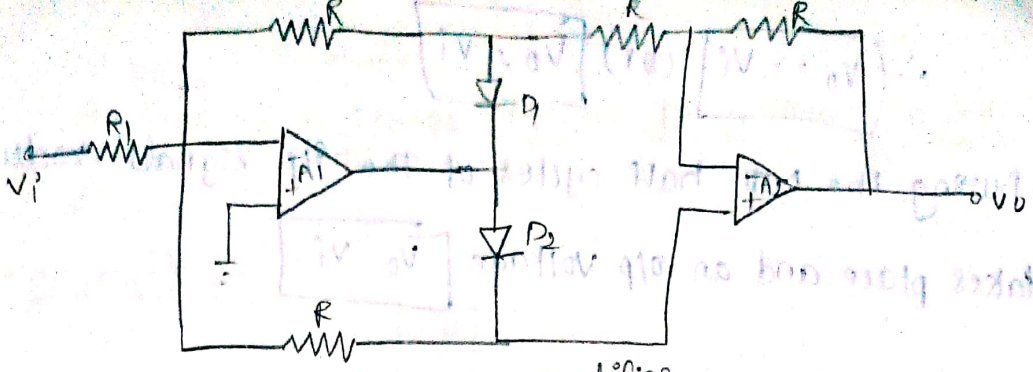
→ The ckt of precision halfwave rectifier using op-amp is shown in fig.

→ The ckt uses two diodes D_1 and D_2 The resistor R_2 to the F.B path the resistor R_1 in the i/p ckt.

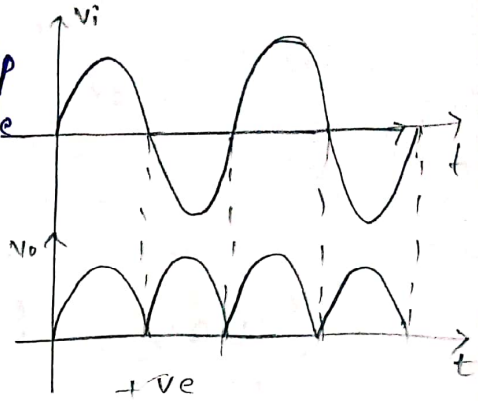
Since the noninverting i/p terminal is grounded



→ During the +ve half cycle of the i/p voltage V_i we can see that the diode D_1 gets F.B. The diode D_2 gets R.B. Hence only diode D_1 can conduct and there is no current through resistor R_2 then this result the o/p voltage $V_o = 0$.



b. full wave rectifier.



→ During the -ve half cycle of the i/p voltage V_i. It is seen that the diode D_1 gets R.B. and diode D_2 F.B.

Hence D_1 is OFF and D_2 is ON. The ckt behaves like an inverting amp.

→ ∴ The o/p voltage is given by $V_o = -R_2/R_1 V_i$.

→ Let R_2 and R_1 the resistors of equal magnitude i.e, $R_1 = R_2$

$$\therefore V_o = -V_i.$$

→ But During the -ve half cycle V_i itself -ve

$$\therefore V_o = V_i.$$

→ The i/p and o/p waveforms on shown in figure.

precision fullwave rectifiers:

→ precision fullwave rectifier is shown in fig.

→ The ckt uses two identical diodes D_1 and D_2 and several resistors in conjuction with two op-amps as shown in fig

→ During the +ve half cycle of the i/p voltage V_i. The diode D_1 gets F.B, and D_2 gets R.B.

→ ∴ The o/p voltage $V_o = V_i$.

→ Illy During the -ve half cycle of the i/p voltage V_i the diode D_1 gets R.B, and D_2 gets F.B.

$\therefore$ $V_o = -V_i$ (or) $V_o = V_i$

→ During the both half cycles of the i/p signals conduction takes place and an o/p voltage $V_o = V_i$