DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE, PERAMBALUR - 621212

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC6601 - VLSI DESIGN

QUESTION BANK

UNIT I - MOS TRANSISTOR PRINCIPLE

PART – A

1. What is Channel-length modulation? *(Apr/May-17, Apr/may-16)*

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied $V_{DS,}$ increasing V_{DS} causes the, depletion region at the drain junction to grow, reducing the length of the effective channel.

2. What is Latch – up? How it can be prevented *(Apr/may-16)*

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DS} and V_{SS} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

- ✓ An increase in substrate doping levels with a consequent drop in the value of Rpsubs.
- ✓ Reducing Rnwell by control of fabrication parameters and ensuring a low contact resistance to VDD.
- ✓ By introducing guard rings.

3. What is body effect in MOSFETs? Or Define body bias effect. *(Nov/Dec-16, Nov/Dec-13)*

The threshold voltage VT is not a constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This effect is called the body effect or substrate bias effect.

4. Define propagation delay of CMOS Inverter. *(Apr/May-17)*

The inverter propagation delay (t_P) is defined as the average of the low-to-high (t_{PLH}) and the high-to low (t_{PHL}) propagation delays: $tp = \frac{t_{PHL} + t_{PLH}}{2}$.

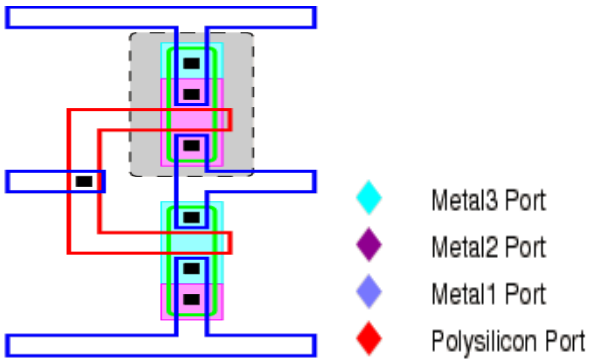
Propagation delays t_{PLH} and t_{PHL} are defined as the times required for output voltage to reach the middle between the low and high logic levels, i.e. 50 % of V_{DD} in our case of CMOS logic.

5. Define the Lambda design rules used for layout? *(May/Jun-13, Apr/may-15)*

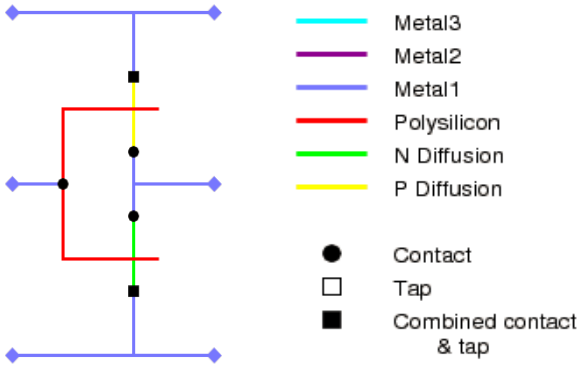
Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

6. Draw the stick diagram and layout for CMOS Inverter. ***(Nov/Dec-16)***

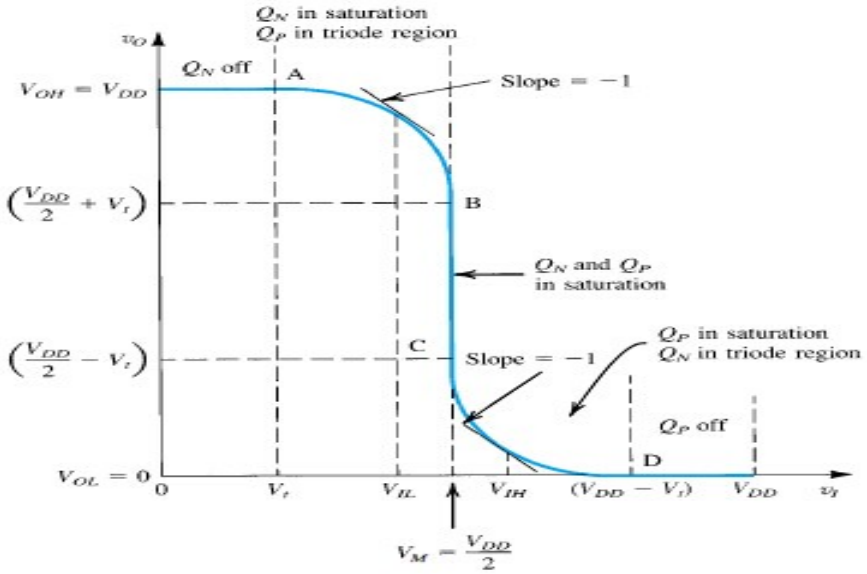
Layout for CMOS Inverter:



Stick diagram for CMOS Inverter:



7. Draw the DC transfer characteristics of CMOS inverter. ***(Apr/may-15, Nov/Dec-13)***



8. What is the need for design rules? ***(Nov/Dec-14)***

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.

9. Define any two layout design rules. ***(Nov/Dec-15, May/Jun-14)***

Micron design rule:

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

Lambda design rule:

Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

10. Why nMOS transistor is selected as pull down transistor. ***(Nov/Dec-17)***

When high voltage is given at the input nMOS is turned ON. So the output is pulled down to Vss. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VTp| — the PMOS turns off at that point, and stops contributing dis-charge current. NMOS transistors are hence the preferred devices in the PDN.

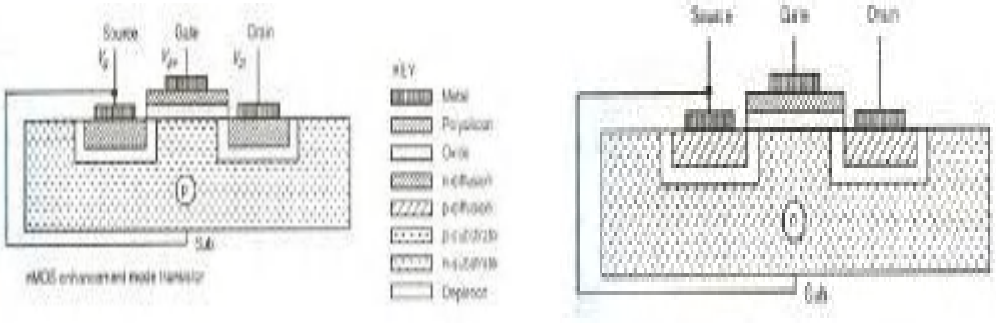
PART –B (Answers as Hint)

1. Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics. ***(May/Jun-16, Nov/Dec-14, May/Jun-13)***

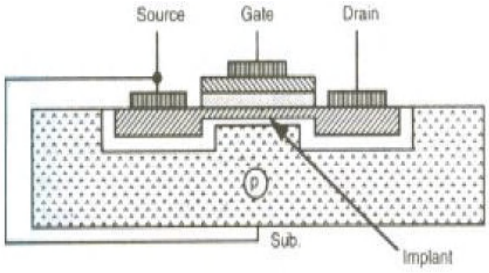
- **<u>Basic MOS Transistors operation:</u>** ***<u>(4 Marks)</u>***

We have two types of FETs. They are Enhancement mode and depletion mode transistor. Also we have PMOS and NMOS transistors.

(i) In **Enhancement mode transistor** channel is going to form after giving a proper positive gate voltage. We have NMOS and PMOS enhancement transistors.



(ii) In **Depletion mode transistor** channel will be present by the implant. It can be removed by giving a proper negative gate voltage. We have NMOS and PMOS depletion mode transistors.



- **<u>Three regions of operation of a MOS transistor</u>** ***<u>(4 Marks)</u>***

a) Vgs > Vt Vds = 0 Since Vgs > Vt and Vds = 0 the channel is formed but no current flows between drain and source.

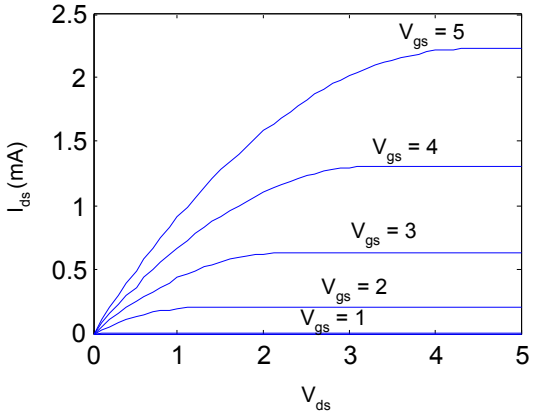
b) Vgs > Vt Vds < Vgs - Vt This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased and the channel starts to pinch. This is called as the pinch off point.

c) Vgs > Vt Vds > Vgs - Vt This region is called Saturation Region where the drain current remains almost constant. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current. The typical threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd.

- **Derivation:** ***(6 Marks)***

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

- **Draw the VI characteristics** ***(2 Marks)***



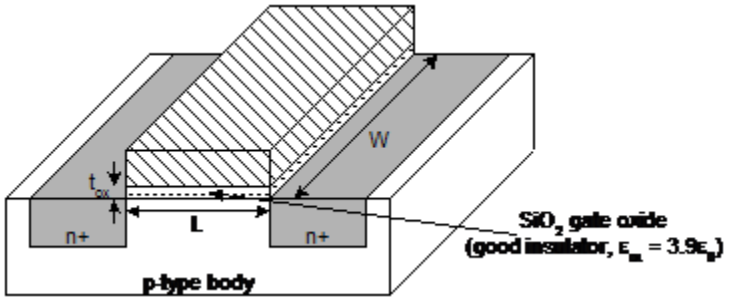
2. Explain in detail of C-V characteristics of MOSFET. ***(Nov/Dec-15)***

- **Simple MOS capacitance model** ***(4 Marks)***

  Approximate channel as connected to source

  $C_{gs} = e_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W$

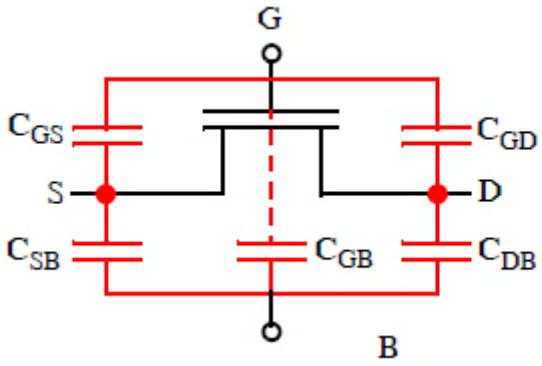
  $C_{permicron}$ is typically about 2 fF/mm



- **Detailed MOS capacitance model** ***(4 Marks)***

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Linear	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

- **MOS device capacitance *(4 Marks)***



$C_{GS} = C_{gs} + C_{gsO}$
$C_{GD} = C_{gd} + C_{gdO}$
$C_{GB} = C_{gb}$
$C_{SB} = C_{Sdiff}$
$C_{DB} = C_{Ddiff}$

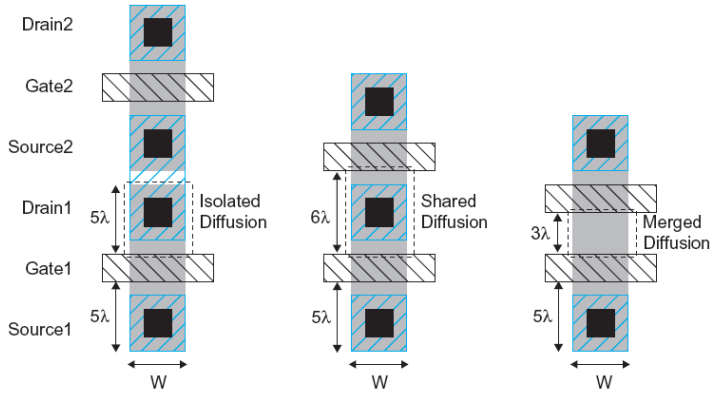
- **Diffusion capacitance *(4 Marks)***

C_{sb}, C_{db}

Undesirable, called *parasitic* capacitance

Capacitance depends on area and perimeter

- ✓ Use small diffusion nodes
- ✓ Comparable to C_g for contacted diff
- ✓ ½ C_g for un contacted
- ✓ Varies with process



3. Discuss the mathematical equations that can be used to model the drain current and diffusion capacitances of MOS transistor. *(Nov/Dec-16)*

- **Drain current derivation: *(8 Marks)***

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

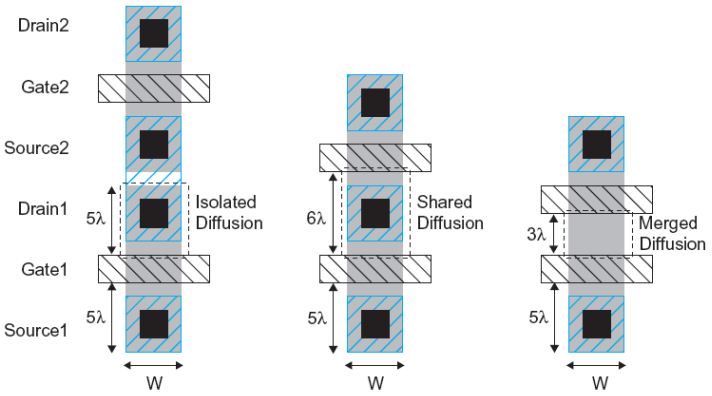
- **Diffusion capacitances of MOS transistor: *(8 Marks)***

C_{sb}, C_{db}

Undesirable, called *parasitic* capacitance

Capacitance depends on area and perimeter

- ✓ Use small diffusion nodes
- ✓ Comparable to C_g for contacted diff
- ✓ ½ C_g for un contacted
- ✓ Varies with process



4. Explain the electrical properties of MOS transistor in detail. *(Nov/Dec-17, Nov/Dec-13)*

- **<u>Ideal IV characteristics *(4 Marks)*</u>**

  Three regions of operation

  - ✓ Cutoff *(1 Mark)*
  - ✓ Linear *(1 Mark)*
  - ✓ Saturation *(1 Mark)*
  - ✓ Equation *(1 Mark)*
- **<u>Non ideal characteristics *(4 Marks)*</u>**
  - High Field Effects *(1 Mark)*
    - ✓ Mobility Degradation
    - ✓ Velocity Saturation
  - Channel Length Modulation*(1 Mark)*
  - Threshold Voltage Effects*(1 Mark)*
    - ✓ Body Effect
    - ✓ Drain-Induced Barrier Lowering
    - ✓ Short Channel Effect
  - Leakage*(1 Mark)*
    - ✓ Subthreshold Leakage
    - ✓ Gate Leakage
    - ✓ Junction Leakage
- **<u>C-V characteristics *(4 Marks)*</u>**
  - ✓ Simple MOS capacitance model *(1 Mark)*
  - ✓ Detailed MOS capacitance model *(4 Mark)*
  - ✓ MOS device capacitance *(4 Mark)*
  - ✓ Diffusion capacitance *(4 Mark)*

5. Explain the need of scaling, scaling principles and fundamental units of CMOS inverter. *(Nov/Dec-17, Apr/May-17)*

- **Need of scaling: *(8 Marks)***

  Definition: *(2 Marks)*

  Proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the dev ice, result in a dev ice either *larger* o r *smaller* than the u n -sea led device.

  Factors: *(6 Marks)*

  - ✓ Consider 2 scaling factors, α and β
  - ✓ 1/ β is the scaling factor for VDD and oxide thickness D
  - ✓ 1/ α is scaling factor for all other linear dimensions
  - ✓ We will assume electric field is kept constant

  It is important that you understand how the following parameters are affected by scaling

  - ✓ Gate Area, Gate Capacitance per unit area, Gate Capacitance
  - ✓ Charge in Channel, Channel Resistance
  - ✓ Transistor Delay, Maximum Operating Frequency
  - ✓ Transistor Current, Switching Energy
  - ✓ Power Dissipation Per Gate (Static and Dynamic)
  - ✓ Power Dissipation Per Unit Area
  - ✓ Power - Speed Product

- **Scaling Principles and Fundamental units: *(8 Marks)***

  The Reliability Bathtub Curve, Its Origin and Implications

  - ✓ Key Reliability Functions and Their Use in Reliability Analysis
  - ✓ Defect Screening Techniques and Their Effectiveness
  - ✓ Accelerated Testing and Estimation of Useful Operating Life
  - ✓ Reliability Data Collection and Analysis in Integrated Circuits
  - ✓ Past Technology Scaling Trends
  - ✓ Forward Looking Projections with a Focus on Examining and Understanding of the Impact on VLSI Reliability
  - ✓ Power Density Trends: Operating temperature, activation energies for dominant VLSI failure mechanisms, and reliability impact
  - ✓ Reliability Strategies In Fables Environments

6. Discuss the principle of constant field and lateral scaling. And write the effects of the above scaling methods on the device characteristics. *(May/Jun-16, Nov/Dec-15)*

- **Constant field or Full scaling:*(8 Marks)***

Definition: *(2 Marks)*

All dimensions scaled by same factors keeping the electric field as constant.

Explanation: *(2 Marks)*

- ✓ All the lengths (L G, Z, dOX) and voltages (VDS, VGS, Vth) are scaled by same factor k
- ✓ Electric field unchanged
- ✓ Punch through effect
- ✓ Sol: Increase doping of acceptor by same factor, k (Scaling of Depletion widths)

Effects of scaling: *(4 Marks)*

The effects of constant field scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (1) – (6).

Gate oxide capacitance per unit area, $C'ox = \varepsilon ox/t'ox$

$= S. \varepsilon ox/tox$

$= S.Cox$ ----------(1)

Transconductance, $k'n = \mu n.C'ox.W'/L' = S. kn$ ----------(2)

Drain current, $I'D (lin) = k'n/2.[2.(V'GS-V'TH).V'DS – V'^2DS]$

$= S. kn/2. 1/S^2.[2.(VGS-VTH).VDS – V^2DS]$

Hence, $I'D (lin) = ID (lin)/S$ ----------(3)

$I'D (sat) = k'n/2. (V'GS-V'TH)^2$

$= S. kn/2. 1/S^2. (VGS-VTH)^2$

Hence, $I'D (sat) = ID (Sat)/S$ ----------(4)

Power dissipation, $P'= I'D . V'DS$

$= 1/S^2 . ID . VDS$

Hence, $P'= P/S^2$ ----------(5)

Power dissipation density, $P'_d = P'/ (W'. L') = P_d$ ----------(6)

- **Lateral scaling or General scaling: *(8 Marks)***

Definition: *(2 Marks)*

Gate length is scaled. It is applied when dimensions and voltages are scaled independently using two variables as S & U.

Explanation: *(2 Marks)*

Effects of scaling: *(4 Marks)*

The effects of constant voltage scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (7) – (12).

Gate oxide capacitance per unit area, $C'ox = \varepsilon ox/t'ox$

$= S. \varepsilon ox/tox$

$= S.Cox$ ----------(7)

Transconductance, $k'n = \mu n.C'ox.W'/L' = S. kn$ ----------(8)

Drain current, $I'_D (lin) = k'n/2. [2.(V'_{GS}-V'_{TH}).V'_{DS} – V'^2_{DS}]$

$= S. kn/2. [2.(V_{GS}-V_{TH}).V_{DS} – V^2_{DS}]$

Hence, $I'_D (lin) = S. ID (lin)$ ----------(9)

$I'_D (sat) = k'n/2. (V'_{GS}-V'_{TH})^2$

$= S. kn/2. (V_{GS}-V_{TH})^2$

Hence, $I'_D(sat) = S. I_D(Sat)$ ----------(10)

Power dissipation, $P' = I'_D . V'_{DS}$

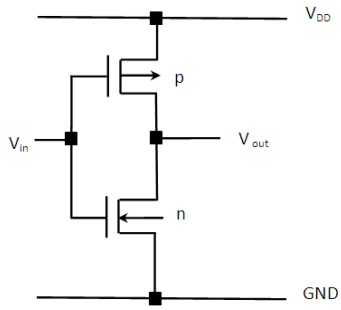
$= S. I_D . V_{DS}$

Hence, $P' = S. P$ ----------(11)

Power dissipation density, $P'd = P'/ (W'. L') = S^3 . Pd$ ----------(12)

7. Draw and explain the D.C and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation. *(Apr/May-17, May/Jun-16, Apr/May-15, Nov/Dec-15, May/Jun-14, May/Jun-13, Nov/Dec-12)*

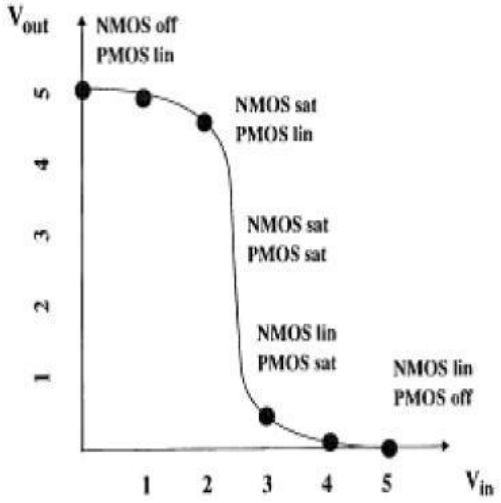
- **CMOS inverter diagram *(2 Marks)***

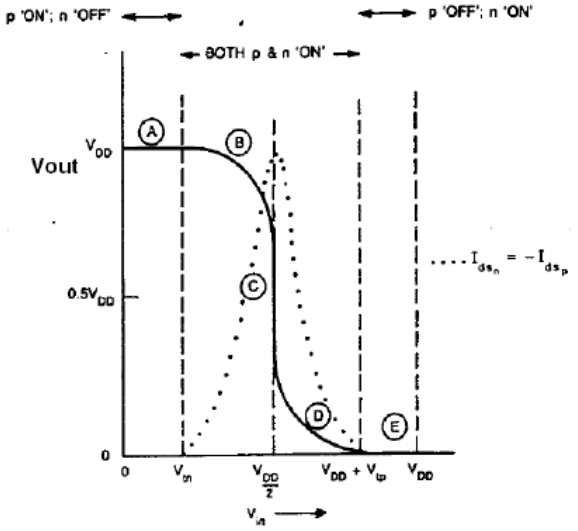


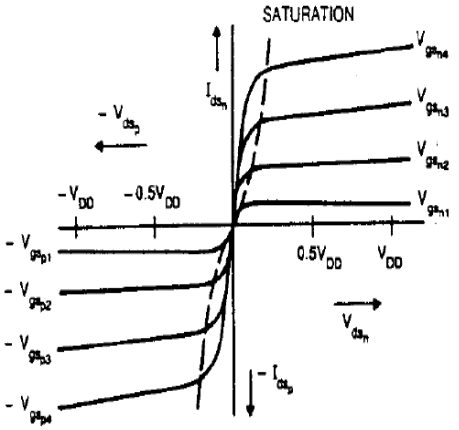
- **Explanation: *(6 Marks)***

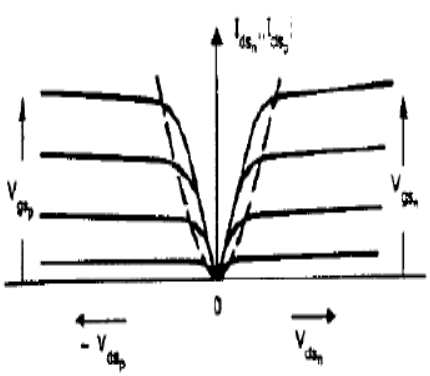
A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal. The operation of the CMOS inverter can be divided into five regions indicated.

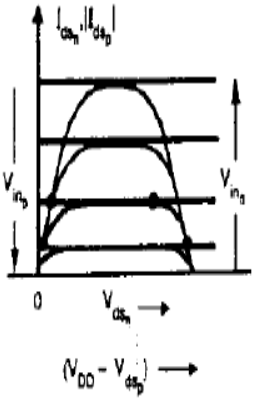
MOSFET	Condition on MOSFET	State of MOSFET
NMOS	Vgs<Vtn	OFF
NMOS	Vgs>Vtn	ON
PMOS	Vsg<Vtp	OFF
PMOS	Vsg>Vtp	ON











- **Regions with formula:** ***(8 Marks)***

Region A: P device is OFF and n device is ON. Vout=VDD.

Region B: PMOS is linear region and NMOS is saturation region.

Region C: Both n and p transistors are in saturation region.

Region D: PMOS is saturation region and NMOS is linear region.

Region E: The output in this region is zero because the P device is OFF and n device is ON.

REGION	CONDITION	p-DEVICE	n-DEVICE	OUTPUT
A	$0 \leq V_{in} \leq V_{tn}$	linear	cut-off	$V_O = V_{DD}$
B	$V_{tn} \leq V_{in} < \frac{V_{DD}}{2}$	linear	saturated	$^*V_O = (V_{in} + 1) - \sqrt{15 - 6V_{in}}$
C	$V_{in} = \frac{V_{DD}}{2}$	saturated	saturated	$V_O \neq f(V_{in})$
D	$\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - V_{tp}$	saturated	linear	$^*V_O = (V_{in} - 1) - \sqrt{6V_{in} - 15}$
E	$V_{in} \geq V_{DD} - V_{tp}$	cut-off	linear	$V_O = 0$

8. (i) Explain in detail about the body effect and its effect in MOS device. ***(May/Jun-16, May/Jun-13)***

- **Definition:** ***(2 Marks)***

Body effect refers to the change in the transistor threshold voltage (VT) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the VT, the body can be thought of as a second gate that helps determine how the transistor turns on and off.

- **Equations:** ***(6 Marks)***

V_{sb} affects the charge required to invert the channel

- Increasing V_s or decreasing V_b increases V_t $\quad V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$

f_s = *surface potential* at threshold $\quad \phi_s = 2v_T \ln\frac{N_A}{n_i}$

- Depends on doping level N_A
- And intrinsic carrier concentration n_i

γ = *body effect coefficient* $\quad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$

For small source-to-body voltage, treat as linear

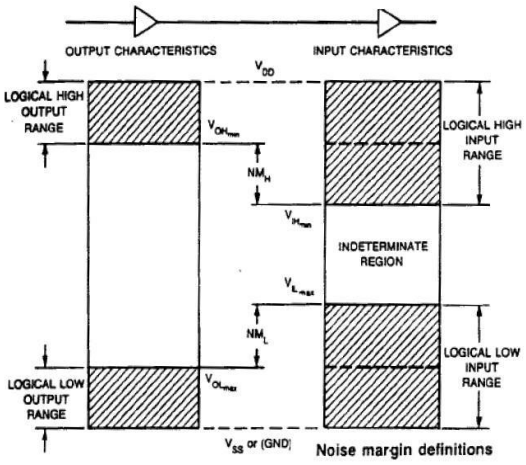
$$V_t = V_{t0} + k_\gamma V_{sb} \qquad k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si}N_A}{v_T \ln\frac{N_A}{n_i}}}}{2C_{ox}}$$

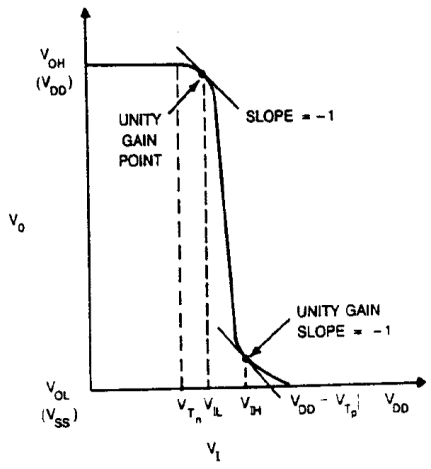
(ii) Derive the noise margins for CMOS inverter. ***(Nov/Dec-16)***

Definition and Types: ***(4 Marks)***

Noise Margin: Noise margin is a parameter related to input output characteristics. It determines the allowable noise voltage on the input so that the output is not affected. We will specify it in terms of two things: LOW noise margin HIGH noise margin.

Diagram and Explanation: ***(6 Marks)***





LOW noise margin: is defined as the difference in magnitude between the maximum Low output voltage of the driving gate and the maximum input Low voltage recognized by the driven gate.
NML=|VILmax – VOLmax|

HIGH noise margin: is defined difference in magnitude between minimum High output voltage of the driving gate and minimum input High voltage recognized by the receiving gate.
NMH=|Vohmin – VIHmin|

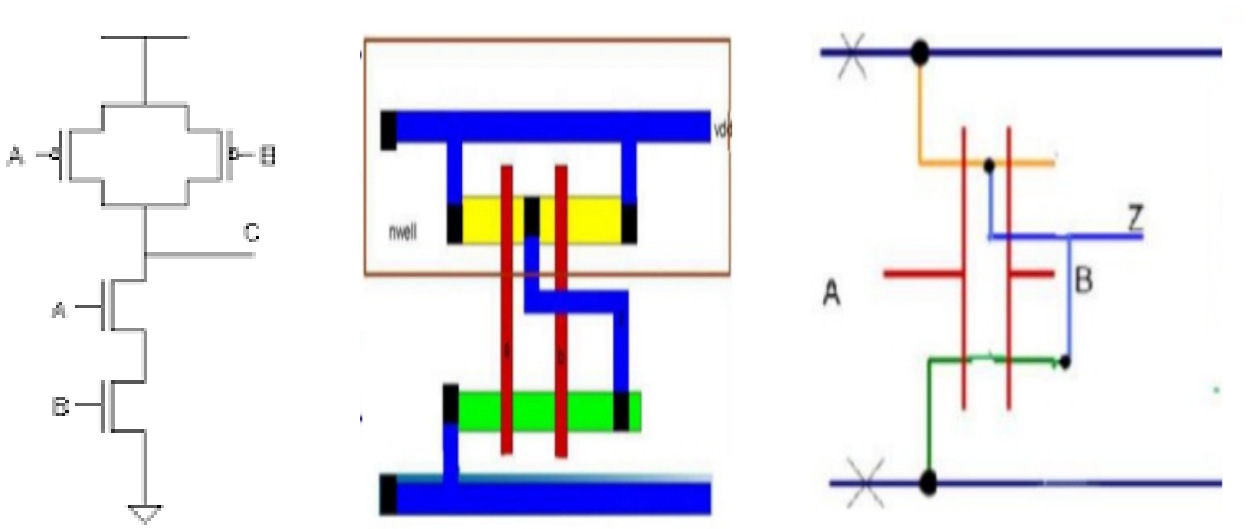
9. (i) Write the layout design rules and Draw the layout diagram for NAND and NOR gate. ***(Nov/Dec-17, Apr/May-17)***

- **Design Rules:** ***(4 Marks)***

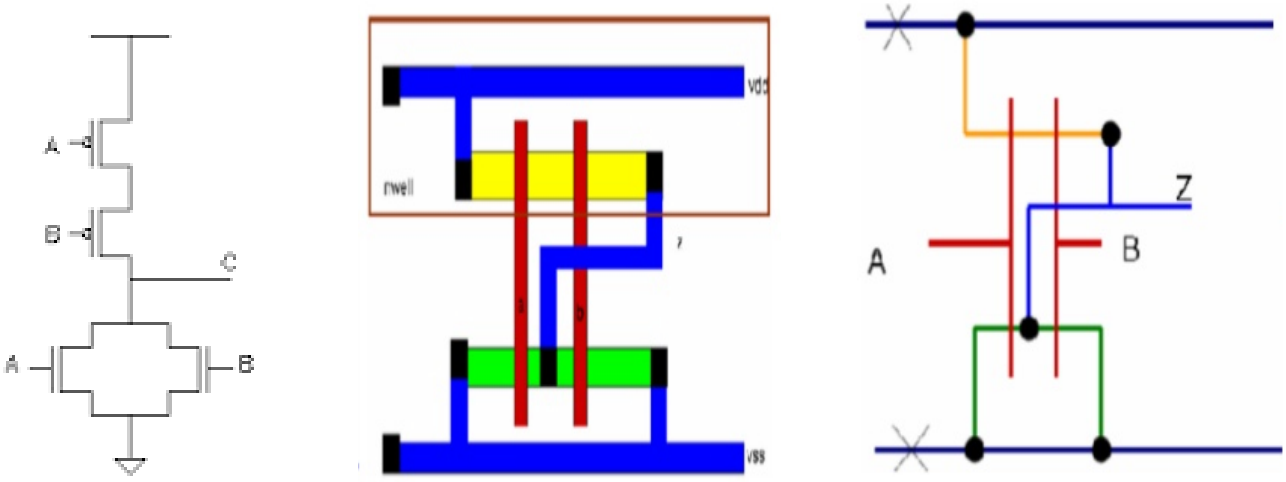
Design rules represent a tolerance that ensures high probability of correct fabrication - rather than a hard boundary between correct and incorrect fabrication.

- ✓ Micron design rule *(1 Mark)*
- ✓ Lambda design rule*(1 Mark)*

- **Layout diagram for NAND gate:** ***(2 Marks)***

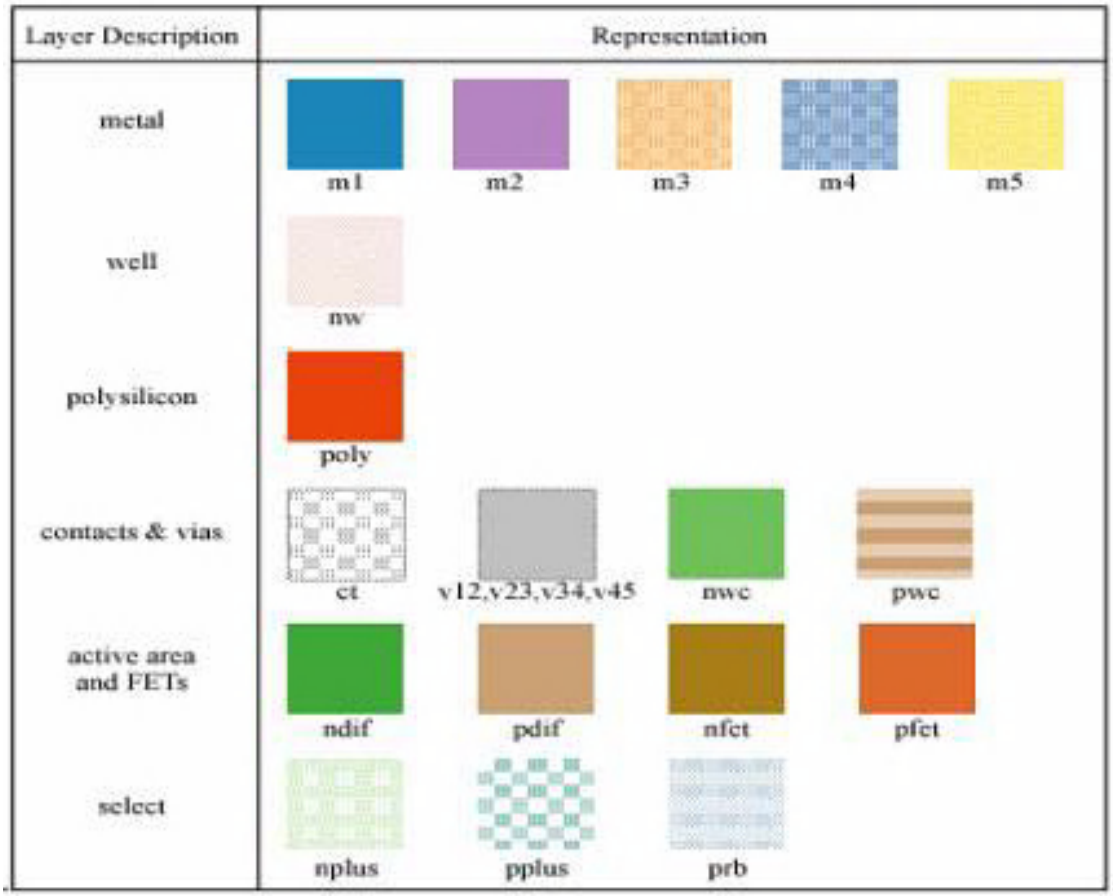


- **Layout diagram for NOR gate:** ***(2 Marks)***

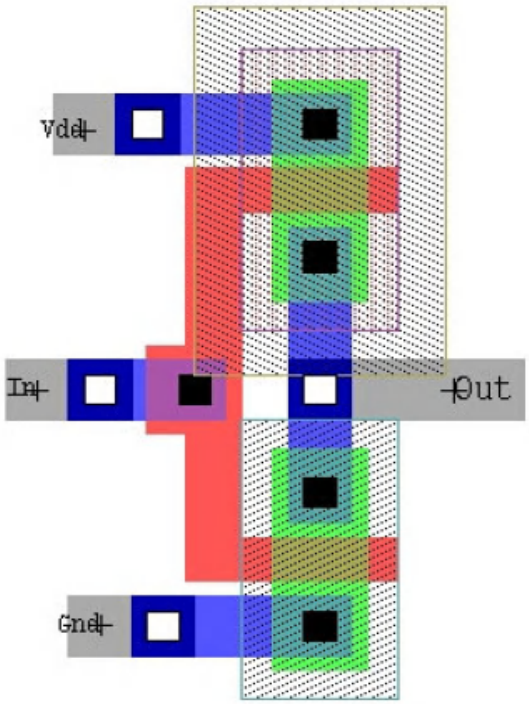


(ii) Discuss in detail with a neat layout, the design rules for a CMOS inverter. ***(Nov/Dec-16)***

- **Layout rules:** ***(4 Marks)***



- **CMOS inverter:** ***(4 Marks)***



10. Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. ***(Nov/Dec-16, Apr/May-15, Nov/Dec-12)***

- **Definition:** ***(2 Marks)***

  The n-well process is that it can be fabricated on the same process line as conventional n MOS. n –well CMOS circuits are also superior to p-well because of the lower substrate bias effects on transistor threshold voltage and inherently lower parasitic capacitances associated with source and drain regions.

- **Explanation of each steps:** ***(14 Marks)***