DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE

PERAMBALUR-621212

COURSE PLAN (2022 – 2023 ODD SEMESTER)

Name of the Faculty				
Designation/Department	Assistant Professor / ECE			
Course Code/Name	U20EC505/ Communication Networks And Architecture			
Year/Section/Department	III/ECE A&B			
Credits Details	L:3	T: 0	P: 0	C:3
Total Contact Hours Required	45			

Syllabus:

UNIT I	**FUNDAMENTALS & LINK LAYER**	**9**
Overview of Data Communications, Networks , Building Network and its types, Overview of Internet , Protocol Layering , OSI Model , Physical Layer , Overview of Data and Signals ,introduction to Data Link Layer ,Link layer Addressing, Error Detection and Correction		
UNIT II	**MEDIA ACCESS & INTERNETWORKING**	**9**
Overview of Data link Control and Media access control, Ethernet (802.3) , Wireless LANs ,Available Protocols, Bluetooth, Bluetooth Low Energy, Wi-Fi ,6LowPAN,Zigbee, Network layer services, Packet Switching, IPV4 Address, Network layer protocols (IP, ICMP, Mobile IP).		
UNIT III	**ROUTING**	**9**
Routing, Unicast Routing, Algorithms, Protocols, Multicast Routing and its basics, Overview of Intradomain and interdomain protocols, Overview of IPv6 Addressing , Transition from IPv4 to IPv6.		
UNIT IV	**COMPUTER ORGANIZATION & INSTRUCTIONS**	**9**
Basics of a computer system: Evolution, Ideas, Technology, Performance, Power wall, Uni-processors to Multiprocessors. Addressing and addressing modes. Instructions: Operations and Operands, Representing instructions, Logical operations, control operations.		
UNIT V	**ARITHMETIC AND PROCESSOR OPERATION**	**9**
Fixed point Addition, Subtraction, Multiplication and Division. An Overview of Pipelining - Pipelined Data path and Control. Memory hierarchy, Memory Chip Organization, Cache memory, Virtual memory.		

Objective:

- Understand the division of network functionalities into layers.
- Be familiar with the components required to build different types of networks.
- Be exposed to the required functionality at each layer.
- Learn the flow control and congestion control algorithms.

Text Book:

1. Behrouz A. Forouzan, Data communication and Networking, 5th Edition, Tata McGrawHill, 2013.
2. David A. Patterson and John L. Hennessey, Computer Organization and Design,5th edition, Morgan Kauffman / Elsevier, 2014.
3. William Stallings, Computer Organization and Architecture, Designing for Performance,10th Edition, Pearson Education, 2017.

Reference Book:

1. Govindarajalu, Computer Architecture and Organization - Design Principles and Applications, 2nd edition, McGraw-Hill Education India Pvt Ltd, 2014.
2. James F.Kurose, Keith W.Ross, Computer Networking - A Top-Down Approach Featuring the Internet, 7th Edition, Pearson Education, 2016.
3. Miles J. Murdocca and Vincent P. Heuring, Computer Architecture and Organization: AnIntegrated approach, 2nd edition, Wiley India Pvt Ltd, 2015.
4. Nader. F. Mir, Computer and Communication Networks, Pearson Prentice HallPublishers, 2nd Edition, 2014.

Website:

W1. http://www.youtube.com/watch?v=-6Uoku-M6oY **(ISO/OSI layers)**

W2. http://nptel.ac.in/courses/106105081 **(Computer network)**

Online Mode of Study (if Any):

- Error detection
- Flow control

- ❖ Flow control and retransmission

Course Plan:

Topic No.	Topic	Books for Reference	Page No.	Teaching methodology	No. of periods Required	Cumulative No. of. Periods
UNIT I	**FUNDAMENTALS AND LINK LAYER**					**(9)**
1	Introduction, Building a network	T1	1-5	BB	1	1
2	Requirements	T1	6-20	BB	1	2
3	Layering and protocols	T1,R1	24-32	BB	1	3
4	Internet architecture	T1	33-35	BB	1	4
5	Network software, Performance	T1	36-38, 44-53	BB	1	5
6	Link layer services	T1	81-90	BB	1	6
7	Framing	T1	91-118	BB	1	7
8	Error detection	T1,R1	91-118	BB	1	8
9	Flow control	T1	91-118	BB	1	9
Outcome of Unit I ● CO1 - Identify the components required to build different types of networks.						
UNIT II	**MEDIA ACCESS AND INTERNETWORKING**					**(9)**
10	Introduction	T1	119	BB	1	10
11	Media access control Ethernet (802.3)	T1	120-127	BB	1	11
12	Wireless LAN, 802.11	T1	128-140	BB	1	12
13	Bluetooth	T1	142-144	BB	1	13
14	Switching and bridging	T1	170-185	BB		14
15	IP,CIDR	T1	203-220	BB	1	15
16	ARP	T1	228-230	BB	1	16
17	DHCP	T1	231-234	BB	1	17

18	ICMP	T1	235	BB	1	18
Outcome of Unit II ● CO2 - Choose the required functionality at each layer for given application						
UNIT III		**ROUTING**				**(9)**
19	Introduction, Routing	T1	240	BB	1	19
20	DVRP, OSPF	T1	242-265	BB	1	20
21	Switch basics	T1	267-270	BB	1	21
22	Global internet	T1	308-310	BB	1	22
23	BGP	T1	313-323	BB	1	23
24	IPV6	T1	324-337	BB	1	24
25	Multicast address	T1	349	BB	1	25
26	Multicast routing ,PIM	T1	341	BB	1	26
27	IPV4	T1	343	BB	1	27
Outcome of Unit III CO3- Identify solution for each functionality at each layer						
UNIT IV		**COMPUTER ORGANIZATION & INSTRUCTIONS**				**(9)**
28	Basics of a computer system: Evolution	T2	13-24	BB	1	28
29	Ideas, Technology, Performance	T2	24-40	BB	1	29
30	Power wall, Uniprocessors to multiprocessors	T2	40-43	BB	1	30
31	Addressing and addressing modes	T2	111	BB	2	32
32	Instructions	T2	62	BB	1	33
33	Operations & operands	T2	63	BB	1	34
34	Representing instructions, Logical operations	T2	80-87	BB	1	35
35	control operations	T2	87-90	BB	1	36
Outcome of Unit IV ● CO4- Discuss about implementation schemes of control unit and pipeline performance.						
UNIT V		**ARITHMETIC AND PROCESSOR OPERATION**				**(9)**
36	Fixed point Addition	T2,T3	178-182	BB	1	37
37	Subtraction	T2	178-182	BB	1	38
38	Multiplication & Division	T2	183-189	BB	1	39
39	Pipelining, Pipelined data path and control	T2	286-303	BB	1	40

40	Memory hierarchy, Memory Chip Organization	T2,T3	703	BB	1	41
41	Cache memory, Virtual memory	T2	706-712	BB	1	42
42	Parallel Bus Architectures, Internal Communication Methodologies	T3	718-726	BB	1	43
43	Serial Bus Architectures, Mass storage	T3	744-750	BB	1	44
44	Input and Output Devices	T3	781-752	BB	1	45

Outcome of Unit V

CO5: Explain the concept of various memories, interfacing and organization of multiple processors.

Course Outcome:

At the end of course, Students should be able to do:

CO1: Identify the components required to build different types of networks.

CO2: Understand the protocols for user applications.

CO3: Describe data representation, instruction formats and the operation of a digital computer.

CO4: Discuss about implementation schemes of control unit and pipeline performance.

CO5: Explain the concept of various memories, interfacing and organization of multiple processors.

Course Outcome Vs Program Outcome Mapping:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO 1	2	0	3	0	0	0	0	0	0	3	0	0
CO 2	2	0	2	0	1	0	0	0	0	2	1	0
CO 3	2	0	2	0	0	0	0	0	0	2	1	0
CO 4	2	0	0	0	0	2	0	0	0	0	1	0
CO 5	2	0	0	0	0	2	0	0	0	0	1	0

Content beyond Syllabus:

- Terminal Emulation (TELNET)
- Groupware(Video Conferencing, Chatting)

Assignment:

Assignment	Batch Details	Register Number	Total Number	Mode of Assignment MCQ/Seminar/PPT	Topics
I	Batch - I	DSUG20106046 to DSUG20106060	15	Seminar	Error Detection & Flow Control
	Batch - II	DSUG20106062 to DSUG20106303	14	PPT	Media access control Ethernet (802.3), Wireless LAN, 802.11
	Batch - III	DSUG20106304 to DSUG20106316	14	Written	Routing
II	Batch - I	DSUG20106046 to DSUG20106060	15	Written	Memory Techniques
	Batch - II	DSUG20106062 to DSUG20106303	14	Seminar	IPV4 & IPV6
	Batch - III	DSUG20106304 to DSUG20106316	14	PPT	Operations & operands
III	Batch - I	DSUG20106046 to DSUG20106060	15	PPT	Addressing and addressing modes
	Batch - II	DSUG20106062 to DSUG20106303	14	Written	Problems in Arithmetic Operations
	Batch - III	DSUG20106304 to DSUG20106316	14	Seminar	Cache memory, Virtual memory

SIM Questions:

SIM 1	1. Discuss in detail about the data link layer functions with neat diagram 2. What is the need for error detection? Explain with example 3. Discuss in detail about the network performance measures 4. Explain the Address Resolution Protocol with an example. 5. Draw the OSI network architecture and explain the functionalities OS each layer in detail. 6. Write the Sliding Window Algorithm and explain it in detail. 7. Compare Stop and Wait ARQ scheme with sliding window ARQ scheme. 8. Write in detail about the flow control mechanisms. 9. Explain in detail i)PPP ii) HDLC 10. Explain the working of DHCP protocol with its header format 11. lustrate the fragmentation and reassembly process in IP with example 12. Explain the Algorithm used for reliable transmission and Flow control.
SIM 2	1. Write notes on the following (i) Internet protocol. (ii) Routers. 2. Discuss in detail about the DIM . 3. Concepts 4. Elaborate in detail about the transition from IPv4 to IPv6. 5. What are the different approaches in Packet Switching? Explain them in detail 6. Discuss in detail about the various Mobile IP concepts. 7. Explain the Multicast Routing Techniques. 8. Discuss in detail about the various routing techniques. 9. i)Discuss in detail about Eight great ideas of computer Architecture.(8) ii) Explain in detail about Technologies for Building Processors and Memory\ 10. i)Discuss the Logical operations and control operations of computer ii)Write short notes on Power wall 11. Explain operations and operands of computer Hardware in detail 12. Define Addressing mode and explain the basic addressing modes with an example for each 13. Explain the various Addressing Techniques.

SIM 3	1. Describe the basic structure of the pipeline processor and explain how it carried out in floating point adder 2. Discuss the various Control Operations. 3. Describe piping techniques used in cache memories. 4. Explain the concept of virtual memory with any one virtual memory management technique. 5. Describe the performance consideration of cache memory. 6. State and explain the rules in arithmetic operations 7. Discuss in detail about division algorithm in detail with diagram and examples 8. Explain the Multiplication algorithm in detail with diagram and examples 9. Explain the Serial Bus Architectures in Detail. 10. Describe the Flynn's Classification in Detail. 11. Explain the Various Mapping Function in Cache Memory. 12. Explain the Parallell Bus Architectures in Detail.

Submission Details:

Phase 1(Before AT 1)		Phase 2 (Before AT 2)		Phase 3 (Before AT 3)	
Assignment 1	**SIM 1**	**Assignment 2**	**SIM 2**	**Assignment 3**	**SIM 3**

Prepared By **Verified By**

Approved By