DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE
(AUTONOMOUS)
(Approved by AICTE & Affiliated to Anna University, Chennai)
Re-Accredited by NAAC with 'A' Grade
Accredited by NBA for AERO, BME, CSE, ECE, EEE, IT & MECH.
PERAMBALUR-621212, TAMILNADU, INDIA.
Website: www.dsengg.ac.in

COURSE PLAN

Name of the Faculty				
Designation/Department	ASSISTANT PROFESSOR/ECE			
Course Code/Name	U23ECT52/ VLSI AND CHIP DESIGN			
Year/Semester/Department	III/V/ECE-B			
Credits Details	L: 3	T: 0	P: 0	C: 3
Total Contact Hours Required	45			

Syllabus:

UNITI/ MOS TRANSISTOR PRINCIPLES	**9**
MOS logic families (NMOS and CMOS), Ideal and Non Ideal I-V Characteristics, CMOS devices. MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, Technology Scaling, power consumption.	
UNITII/ COMBINATIONAL LOGIC CIRCUITS	**9**
Propagation Delays, stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Static Logic Gates, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.	
UNIT III/ SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES	**9**
Static Latches and Registers, Dynamic Latches and Registers, Pipelines, Non bi stable Sequential Circuits. Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.	
UNIT IV/ DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM	**9**
Arithmetic Building Blocks: Data paths, Adder, Multipliers, Shifters, ALUs, Power and Speed Trade-offs, **Case Study:** Design as a trade-off, Designing Memory and Array Structures: Memory Architectures and Building Blocks, Memory core, Memory Peripheral Circuitry.	
UNITV/ ASIC DESIGN AND TESTING	**9**
Introduction to wafer to chip fabrication process flow. Microchip design process & issues in test and verification of complex chips, embedded cores and SOCs, Fault models, Test coding. ASIC Design Flow, Introduction to ASICs, Introduction to test benches, Writing test benches in Verilog HDL, Automatic test pattern generation, Design for testability, Scan design: Test interface and boundary scan.	

Objective:

- ❖ Understand the fundamentals of IC technology components and their characteristics.
- ❖ Understand combinational logic circuits and design principles.
- ❖ Understand sequential logic circuits and clocking strategies.
- ❖ Understand ASIC Design functioning and design.
- ❖ Understand Memory Architecture and building blocks

Textbooks:

1. Jan M Rabaey, Anantha Chandrakasan, "Digital Integrated Circuits: A Design Perspective", PHI, 2016. (Units II, III and IV).
2. Neil H E Weste, Kamran Eshranghian, "Principles of CMOS VLSI Design: A System Perspective," Addison Wesley, 2009. (Units - I, IV).
3. Michael J Smith , "Application Specific Integrated Circuits", Addison Wesley, (Unit - V)
4. Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis", Second Edition, Pearson Education, 2003. (Unit - V)
5. Parag K.Lala, "Digital Circuit Testing and Testability", Academic Press, 1997, (Unit - V)

Reference Book:

1. D.A. Hodges and H.G. Jackson, "Analysis and Design of Digital Integrated Circuits", International Student Edition, McGraw Hill 1983
2. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
3. Samiha Mourad and Yervant Zorian, "Principles of Testing Electronic Systems", Wiley 2000.
4. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

Supplementary Book:

S1:JohnP.Uyemura,"IntroductiontoVLSIcircuitsandSystems", Wiley-India Edition.
S2:Dr. R.Uma, "VLSI DESIGN", Sri Krishna Publications. (UNIT I-V).

Website:

WR1:http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
WR2: https://www.slideshare.net/RajeshYadav49/amit-floor-planning-ppt

Online Mode of Study:

NPTEL:

- ❖ https://onlinecourses.nptel.ac.in/noc23_ee07/preview
- ❖ https://onlinecourses.nptel.ac.in/noc23_ee29/preview

Course Plan:

Topic Number	Topic	Reference Detail	Page Number	Mode of teaching	Number of Periods Required	Cumulative Period
UNIT I- MOS TRANSISTOR PRINCIPLES						
1	Introduction to MOS Logic Families	T2	2	BB	1	1
2	NMOS Logic Family	T2	1-30	BB	1	2
3	CMOS Logic Family	T2	30-60	BB	1	3
4	Ideal I-V Characteristics of MOSFET	T2	61-80	BB	1	4
5	Non-Ideal I-V Characteristics	T2	80-110	BB	1	5
6	CMOS Device Operation – Static Conditions	T2	111-140	PPT	1	6
7	CMOS Device Operation – Dynamic Conditions	T2	141-180	BB	1	7
8	Technology Scaling	T2	181-215	BB	1	8
9	Power Consumption in MOS Devices	T2	160-180	BB	1	9
Outcome of Unit I: **CO1: In depth knowledge of MOS technology**						
UNITII-MICROWAVESEMICONDUCTORDEVICES						
10	Propagation Delays in CMOS	T1	200-215	BB	1	10
11	Elmore's Delay Model	T1	280-300	BB	1	11
12	Stick Diagrams	T1	240-260	PPT	1	12
13	Layout Diagrams	T1	260-270	BB	1	13
14	Combinational Logic Design Examples	T1	220-285	BB	1	14
15	Static vs Dynamic	T1	240	BB	1	15

	Logic Gates					
16	Pass Transistor Logic (PTL)	T1	230-250	BB	1	16
17	Power Dissipation in CMOS Circuits	T1	210,245	BB	1	17
18	Low Power Design principles.	T1	280-285	BB	1	18
Outcome of Unit II: **CO2: Understand Combinational Logic Circuits and Design Principles**						
UNITIII/ COMBINATIONAL LOGIC CIRCUITS						
19	Static Latches and Registers	T1	60-65	BB	1	19
20	Dynamic Latches and Registers	T1	60	BB	1	20
21	Pipeline Design – Fundamentals	T1	38	BB	1	21
22	Pipeline Design – Advanced	T1	38-40	BB	1	22
23	Non-bi stable Sequential Circuits	T1	50-60	BB	1	23
24	Timing Classification of Digital Systems	T1	1-80	BB	1	24
25	Synchronous Design Principles	T1	2-20	BB	1	25
26	Introduction to Self-Timed (Asynchronous) Circuits	T1	38-60	BB	1	26
27	Design and Analysis of Self-Timed Circuits	T1	38-60	BB	1	27
Outcome of Unit III: **CO3: Understand Sequential Logic Circuits and Clocking Strategies**						
UNIT IV/ DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM						
28	Introduction to Arithmetic Building Blocks & Data Paths	T2	472-480	BB	1	28
29	Adders: Types and Architectures	T2	480-495	PPT	1	29
30	Multipliers: Design Techniques	T2	495-510	BB	1	30
31	Shifters and ALU Design	T2	510-520	BB	1	31
32	Power-Speed-Area Trade-offs in Arithmetic Units	T2	520-530	BB	1	32

33	Case Study: Arithmetic Design Trade-off	T2	529	BB	1	33
34	Designing Memory and Array Structures – Overview	T2	420	PPT	1	34
35	Memory Core Design	T2	430-445	BB	1	35
36	Memory Peripheral Circuits	T2	445-460	BB	1	36
Outcome of Unit IV: **CO4: Understand Memory architecture and building blocks**						
UNIT V/ ASIC DESIGN AND TESTING						
37	Wafer to Chip Fabrication Process Flow	T3	1-20	BB	1	37
38	Microchip Design Flow & Verification Challenges	T3	15	BB	1	38
39	Embedded Cores and SoC Testing Issues	T3	500-550	BB	1	39
40	Fault Models and Test Coding	T3	551	BB	1	40
41	ASIC Design Flow & Introduction to ASIC Types	T3	45-50	BB	1	41
42	Introduction to Test Benches	T3	600-630	BB	1	42
43	Writing Test Benches in Verilog HDL	T3	630-670	BB	1	43
44	Automatic Test Pattern Generation (ATPG)	T3	671	BB	1	44
45	Design for Testability (DFT) and Scan Design	T3	720	BB	1	45
Outcome of Unit V: **CO5 & CO6 : Understand the HDL & Understand the ASIC Design Process and Testing.**						

Course Outcome

At the end of course: Students should be able to do:

CO1: In depth knowledge of MOS technology

CO2:Understand Combinational Logic Circuits and Design Principles

CO3:Understand Sequential Logic Circuits and Clocking Strategies

CO4:Understand Memory architecture and building blocks

CO5:Understand the HDL

CO6:Understand the ASIC Design Process and Testing.

Course Outcome Vs Program Outcome Mapping:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	3	-
CO2	3	3	2	-	-	-	-	-	-	-	-	-	3	2
CO3	3	2	3	-	-	-	-	-	-	-	-	-	2	3
CO4	2	3	3	2	-	-	-	-	-	-	-	-	3	3
CO5	2	2	3	3	3	-	-	-	-	2	-	-	3	3
CO6	2	2	2	3	3	-	-	-	-	2	-	-	3	3
AVG	**2.5**	**2.3**	**2.6**	**2.2**	**3**	**-**	**-**	**-**	**-**	**2**	**-**	**-**	**2.8**	**2.8**

Content beyond Syllabus:

- Testing and Low Power VLSI

Internal Evaluation Components:

Webportal	Assignment	Components	Topic Number with Topic / Unit Details	Relevance to CO
Webportal 1	--	Assessment – I (60)	Unit I and II	CO 1 & CO2
	1	Assignment – Handwritten (20)	4.Ideal and Non Ideal I-V Characteristics	CO 1
	2	Assignment – Poster Presentation / PPT (20)	18.Low Power Design principles	CO2
Webportal 2	--	Assessment – II (60)	Unit III and IV	CO3 & CO4
	3	Seminar (20)	25. Synchronous Design Principles	CO3
	4	Case Study Report (20)	33. Arithmetic Design Trade-off	CO4
Webportal 3	--	Model Exam (75)	Unit I to V	CO1 to CO6
	5	MCQ (15)	Unit I to V	CO1 to CO6
	-	Course Attendance (10)	--	--

Submission Details:

Phase 1(Before AT 1)		Phase 2 (Before AT 2)		Phase 3 (Model)
Assignment 1	**Assignment 2**	**Assignment 3**	**Assignment 4**	**Assignment 5**

Google Class Code Details: III ECE B
Class Name: t4z4maaz

PLAN OF ASSESSMENT TEST –DISTRIBUTION OF MARKS:

TEST	CO- MARK WISE DISTRIBUTION						BLOOM'S LEVEL MARK WISE DISTRIBUTION					
AT-1	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**	**BTL1**	**BTL2**	**BTL3**	**BTL4**	**BTL5**	**BTL6**
AT-2	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**	**BTL1**	**BTL2**	**BTL3**	**BTL4**	**BTL5**	**BTL6**
MODEL	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**	**BTL1**	**BTL2**	**BTL3**	**BTL4**	**BTL5**	**BTL6**

Prepared By **Verified By**

Approved By